CIVIOS LOGIC SELECTION GUIDE

1994





54/74 CMOS LOGIC INTEGRATED CIRCUITS

This product selection guide contains technical information on Harris Semiconductor High Speed 54/74 CMOS Logic Integrated Circuits for commercial, industrial and military applications. It covers Harris' High Speed CMOS Logic HC/HCT Series, AC/ACT Series, BiCMOS Interface Logic FCT Series and CMOS Logic CD4000B Series.

The product guide includes a complete index of types and product selection guides. Four separate product sections provide general technical information for CMOS Logic, High Speed CMOS, Advanced CMOS and FCT BiCMOS logic ICs. A Military Grade/High-Reliability Products section describes Harris' high-reliability integrated circuits that are processed and screened in accordance with military, aerospace and critical industrial applications.

Each of the product sections, in addition to the general index, includes a listing of data sheets available through the Harris AnswerFAX Technical Support system. A list of application notes available through the AnswerFAX system is also included.

For complete, current and detailed technical specifications on any Harris device, please contact the nearest Harris sales, representative or distributor office; or direct literature requests to:

Harris Semiconductor Literature Department P.O. Box 883, MS 53-204 Melbourne, FL 32902 Phone: 1-800-442-7747 Fax: 407-724-7240

See Section 8 for Data Sheets Available on AnswerFAX

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All Harris Semiconductor products are manufactured, assembled and tested under ISO9000 quality system certifications

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CMOS LOGIC ICs

PRODUCT SELECTION GUIDE

FOR COMMERCIAL, INDUSTRIAL AND MILITARY APPLICATIONS

•	
High Speed CMOS Logic - HC/HCT Series	2
Advanced CMOS Logic - AC/ACT Series	3
BiCMOS Interface Logic - FCT Series	4

- CMOS Logic CD4000B Series 5
- Harris Military Grade/High-Reliability Products 6
 - Packaging Information 7

General Information

- **How To Use Harris AnswerFAX 8**
 - Sales Offices 9

TECHNICAL ASSISTANCE

For technical assistance on the Harris products listed in this databook, please contact the Field Applications Engineering staff available at one of the following Harris Sales Offices:

UNITED STATES	
CALIFORNIA	Calabasas 818-878-7950 Costa Mesa 714-433-0600 San Jose 408-985-7322
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CMOS LOGIC ICs

PRODUCT SELECTION GUIDE

GENERAL INFORMATION

	PAGE
LOGIC ORDERING INFORMATION.	1-3
HC/HCT High Speed CMOS Nomenclature	1-3
AC/ACT Advanced CMOS Nomenclature.	1-3
FCT Nomenclature	1-3
CD4000 Nomenclature	1-3
LOGIC SELECTION GUIDE	1-4
HC/HCT Series Data Sheet AnswerFAX Document Listing	1-4
AC/ACT Series Data Sheet AnswerFAX Document Listing	1-7
FCT Series Data Sheet AnswerFAX Document Listing	1-9
CD4000 Series Data Sheet AnswerFAX Document Listing	1-10
HARRIS CMOS LOGIC FAMILIES	1-14
High Speed CMOS (HC/HCT) Logic.	1-14
Advanced CMOS (AC/ACT) Logic	1-14
FCT Bus Interface Devices	1-14
CD4000 Logic	1-14
HC/HCT CMOS Logic Functional Diagrams	1-15
AC/ACT CMOS Logic Functional Diagrams	1-36
FCT CMOS Logic Functional Diagrams.	1-44
CD4000 CMOS Logic Functional Diagrams	1-47



Logic Ordering Information

HC/HCT High Speed CMOS and AC/ACT Advanced CMOS Nomenclature (Example: CD 74 ACT 245E, CD 54 HC 245F)



TEMPERATURE RANGE

74 - Temperature Range:

-55°C to +125°C

54 - Temperature Range:





for Harris Digital Logic IC

Type Designation Up to 5 Digits

HIGH-RELIABILITY SCREENING

- 3A Fully Compliant with MIL-STD-883 (See Note)
- X 160 Hour Burn-In (+125°C)

LOGIC LEVEL

- HC High Speed CMOS Logic CMOS Input Levels
- HCT High Speed CMOS Logic TTL Input Levels
- HCU High Speed CMOS Logic CMOS Input Levels, Unbuffered
- AC Advanced CMOS Logic CMOS Input Levels
- ACT Advanced CMOS Logic TTL Input Levels

PACKAGE DESIGNATION

- E Plastic DIP
- EN Plastic Slim-Line 24 Lead DIP
- F Ceramic Frit-Seal DIP
- M Plastic Surface Mount SOIC
- H Chip
- SM Plastic Shrink SOIC (SSOP)

-55°C to +125°C

FCT Nomenclature (Example: 74 FCT 245 ATE)

XX



TEMPERATURE RANGE



Bus Interface Family: TTL Input Levels

- 74 Standard Temperature Range: 0°C to 70°C
- 54 Extended Temperature Range: -55°C to +125°C

SPEED GRADE

Blank, A - Standard Equivalent to FAST™ AT - 30% Faster Than Standard or Standard Speed for 8xx/29xxx Series, Low

Noise/Low Groundbounce Output

Structure

PACKAGE DESIGNATION

- E Plastic DIP
- EN Plastic Slim-Line 24 Lead DIP
- M Plastic Surface Mount SOIC
- SM Plastic Shrink SOIC (SSOP)

CD4000 Nomenclature (Example: CD4011BE)

Type Designation



4XXXX

SUPPLY VOLTAGE

- A 12V Max
- B 18V Max
- UB 18V Max, Unbuffered

HIGH-RELIABILITY SCREENING

- 3 Non-Compliant with MIL-STD-883 Class B
- 3A Fully Compliant with MIL-STD-883 Class B (See Note)
- X 160 Hour Burn-In (+125°C)

Up to 5 Digits PACKAGE DESIGNATION

- D Ceramic Side Brazed DIP
- E Plastic DIP
- F Ceramic Frit-Seal DIP
- K Ceramic Flatpak
- H Chip

NOTE: Most Harris CMOS Logic ICs are available with burn-in to enhance commercial reliability. This cost-effective approach is provided by the Harris Enhanced Product. Enhanced Product is identified with the suffix "X", e.g., CD74HC/HCT373EX.

HC/HCT Series Data Sheet AnswerFAX Document Listing

СМО	S LOGIC	DESCRIPTION	NUMBER OF LEADS	ANSWERFAX DOCUMENT NUMBER
CD54HC/HCT00	CD74HC/HCT00	Quad 2-Input NAND Gate	14	1464
CD54HC/HCT02	CD74HC/HCT02	Quad 2-Input NOR Gate	14	1647
CD54HC/HCT03	CD74HC/HCT03	Quad 2-Input NAND Gate with Open Drain	14	1832
CD54HC/HCT04	CD74HC/HCT04	Hex Inverter/Buffer	14	1471
CD54HC/HCT08	CD74HC/HCT08	Quad 2-Input AND Gate	14	1549
CD54HC/HCT10	CD74HC/HCT10	Triple 3-Input NAND Gate	14	1551
CD54HC/HCT11	CD74HC/HCT11	Triple 3-Input AND Gate	14	1475
CD54HC/HCT14	CD74HC/HCT14	Hex Inverting Schmitt Trigger	14	1781
CD54HC/HCT20	CD74HC/HCT20	Dual 4-Input NAND Gate	14	1601
CD54HC/HCT21	CD74HC/HCT21	Dual 4-Input AND Gate	14	1782
CD54HC/HCT27	CD74HC/HCT27	Triple 3-Input NOR Gate	14	1648
CD54HC/HCT30	CD74HC/HCT30	8-Input NAND Gate	14	1652
CD54HC/HCT32	CD74HC/HCT32	Quad 2-Input OR Gate	14	1643
CD54HC/HCT42	CD74HC/HCT42	BCD-to-Decimal Decoder (1-to-10)	16	1689
CD54HC/HCT73	CD74HC/HCT73	Dual J-K Flip-Flop with Reset	14	1721
CD54HC/HCT74	CD74HC/HCT74	Dual D Flip-Flop with Set and Reset	14	1476
CD54HC/HCT75	CD74HC/HCT75	Dual 2-Bit Bistable Transparent Latch	16	1666
CD54HC/HCT85	CD74HC/HCT85	4-Bit Magnitude Comparator	16	1770
CD54HC/HCT86	CD74HC/HCT86	Quad 2-Input EXCLUSIVE-OR Gate	14	1644
CD54HC/HCT93	CD74HC/HCT93	4-Bit Binary Ripple Counter	14	1849
CD54HC/HCT107	CD74HC/HCT107	Dual J-K Flip-Flop with Reset	14	1722
CD54HC/HCT109	CD74HC/HCT109	Dual J-K Flip-Flop with Set and Reset	16	1667
CD54HC/HCT112	CD74HC/HCT112	Dual J-K Flip-Flop with Set and Reset	16	1843
CD54HC/HCT123	CD74HC/HCT123	Dual Retriggerable Monostable Multivibrator with Reset	16	1708
CD54HC/HCT125	CD74HC/HCT125	Quad 3-State Buffer	14	1771
CD54HC/HCT126	CD74HC/HCT126	Quad 3-State Buffer	14	1772
CD54HC/HCT132	CD74HC/HCT132	Quad 2-Input NAND Schmitt Trigger	14	1649
CD54HC/HCT137	CD74HC/HCT137	3-to-8-Line Decoder with Latch, Inverting	16	1886
CD54HC/HCT138	CD74HC/HCT138	3-to-8-Line Decoder/Demultiplexer, Inverting	16	1477
CD54HC/HCT139	CD74HC/HCT139	Dual 2-to-4-Line Decoder/Demultiplexer	16	1545
CD54HC/HCT147	CD74HC/HCT147	10-to-4-Line Priority Encoder	16	1773
CD54HC/HCT151	CD74HC/HCT151	8-Input Multiplexer	16	1645
CD54HC/HCT153	CD74HC/HCT153	Dual 4-Input Multiplexer	16	1774
CD54HC/HCT154	CD74HC/HCT154	4-to-16-Line Decoder/Demultiplexer	24	1657
CD54HC/HCT157	CD74HC/HCT157	Quad 2-Input Multiplexer	16	1642
CD54HC/HCT158	CD74HC/HCT158	Quad 2-Input Multiplexer, Inverting	16	1642
CD54HC/HCT160	CD74HC/HCT160	Synchronous BCD Decade Counter, Asynchronous Reset	16	1550
CD54HC/HCT161	CD74HC/HCT161	Synchronous 4-Bit Binary Counter, Asynchronous Reset	16	1550
CD54HC/HCT162	CD74HC/HCT162	Synchronous BCD Decade Counter, Synchronous Reset	16	1550
CD54HC/HCT163	CD74HC/HCT163	Synchronous 4-Bit Binary Counter, Synchronous Reset	16	1550

HC/HCT Series Data Sheet AnswerFAX Document Listing (Continued)

смо	S LOGIC	DESCRIPTION	NUMBER OF LEADS	ANSWERFAX DOCUMENT NUMBER
CD54HC/HCT164	CD74HC/HCT164	8-Bit Serial-In/Parallel-Out Shift Register	14	1658
CD54HC/HCT165	CD74HC/HCT165	8-Bit Parallel-In/Serial-Out Shift Register	16	1672
CD54HC/HCT166	CD74HC/HCT166	8-Bit Parallel-In/Serial-Out Shift Register	16	1501
CD54HC/HCT173	CD74HC/HCT173	Quad D Flip-Flop, Three-State	16	1641
CD54HC/HCT174	CD74HC/HCT174	Hex D-Type Flip-Flop with Reset	16	1608
CD54HC/HCT175	CD74HC/HCT175	Quad D-Type Flip-Flop with Reset	16	1474
CD54HC/HCT181	CD74HC/HCT181	4-Bit Arithmetic Logic Unit	24	1829
CD54HC/HCT190	CD74HC/HCT190	Presettable Synchronous BCD Decade Up/Down Counter	16	1662
CD54HC/HCT191	CD74HC/HCT191	Synchronous 4-Bit Binary Up/Down Counter	16	1662
CD54HC/HCT192	CD74HC/HCT192	Synchronous BCD Decade Up/Down Counter	16	1674
CD54HC/HCT193	CD74HC/HCT193	Synchronous 4-Bit Binary Up/Down Counter	16	1674
CD54HC/HCT194	CD74HC/HCT194	4-Bit Bidirectional Universal Shift Register	16	1668
CD54HC/HCT195	CD74HC/HCT195	4-Bit Parallel Access Shift Register	16	1482
CD54HC/HCT221	CD74HC/HCT221	Dual Monostable Multivibrator with Reset	16	1670
CD54HC/HCT237	CD74HC/HCT237	3-to-8-Line Decoder/Demultiplexer with Address Latches	16	1886
CD54HC/HCT238	CD74HC/HCT238	3-to-8-Line Decoder/Demultiplexer	16	1477
CD54HC/HCT240	CD74HC/HCT240	Octal Buffer Line Driver, Three-State, Inverting	20	1656
CD54HC/HCT241	CD74HC/HCT241	Octal Buffer Line Driver, Three-State	20	1656
CD54HC/HCT242	CD74HC/HCT242	Quad-Bus Transceiver, Three-State, Inverting	14	1488
CD54HC/HCT243	CD74HC/HCT243	Quad-Bus Transceiver, Three-State	14	1488
CD54HC/HCT244	CD74HC/HCT244	Octal-Buffer Line Driver, Three-State	20	1656
CD54HC/HCT245	CD74HC/HCT245	Octal-Bus Transceiver, Three-State	20	1651
CD54HC/HCT251	CD74HC/HCT251	8-Input Multiplexer, Three-State	16	1489
CD54HC/HCT253	CD74HC/HCT253	Dual 4-Input Multiplexer, Three-State	16	1673
CD54HC/HCT257	CD74HC/HCT257	Quad 2-Input Multiplexer, Three-State; Non-Inverting Outputs	16	1650
CD54HC/HCT258	CD74HC/HCT258	Quad 2-Input Multiplexer, Three-State; Inverting Outputs	16	1775
CD54HC/HCT259	CD74HC/HCT259	8-Bit Addressable Latch	16	1727
CD54HC/HCT273	CD74HC/HCT273	Octal D-Type Flip-Flop with Reset	20	1479
CD54HC/HCT280	CD74HC/HCT280	9-Bit Odd/Even Parity Generator/Checker	14	1669
CD54HC/HCT283	CD74HC/HCT283	4-Bit Adder with Fast Carry	16	1848
CD54HC/HCT297	CD74HC/HCT297	Digital Phase-Locker Loop Filter	16	1852
CD54HC/HCT299	CD74HC/HCT299	8-Bit Universal Shift Register Three-State	20	1485
CD54HC/HCT354	CD74HC/HCT354	8-Input Multiplexer/Register, Three-State	20	1690
CD54HC/HCT356	CD74HC/HCT356	8-Input Multiplexer/Register, Three-State	20	1690
CD54HC/HCT365	CD74HC/HCT365	Hex Buffer/Line Driver, Three-State	16	1539
CD54HC/HCT366	CD74HC/HCT366	Hex Buffer/Line Driver, Three-State, Inverting	16	1539
CD54HC/HCT367	CD74HC/HCT367	Hex Buffer/Line Driver, Three-State	16	1538
CD54HC/HCT368	CD74HC/HCT368	Hex Buffer/Line Driver, Three-State, Inverting	16	1538
CD54HC/HCT373	CD74HC/HCT373	Octal Transparent Latch, Three-State	20	1679
CD54HC/HCT374	CD74HC/HCT374	Octal D Flip-Flop, Three-State	20	1663
CD54HC/HCT377	CD74HC/HCT377	Octal D-Type Flip-Flop with Data Enable	20	1675

HC/HCT Series Data Sheet AnswerFAX Document Listing (Continued)

смоѕ	LOGIC	DESCRIPTION	NUMBER OF LEADS	ANSWERFAX DOCUMENT NUMBER
CD54HC/HCT390	CD74HC/HCT390	Dual Decade Ripple Counter	16	1838
CD54HC/HCT393	CD74HC/HCT393	Dual 4-Bit Binary Ripple Counter	14	1653
CD54HC/HCT423	CD74HC/HCT423	Dual Retriggerable Monostable Multivibrator with Reset	16	1708
CD54HC/HCT533	CD74HC/HCT533	Octal Transparent Latch, Three-State; Inverting	20	1599
CD54HC/HCT534	CD74HC/HCT534	Octal D Flip-Flop, Three-State, Inverting	20	1640
CD54HC/HCT540	CD74HC/HCT540	Octal Buffer Line Driver, Three-State, Inverting	20	1659
CD54HC/HCT541	CD74HC/HCT541	Octal Buffer Line Driver, Three-State	20	1659
CD54HC/HCT563	CD74HC/HCT563	Octal Transparent Latch, Three-State, Inverting	20	1599
CD54HC/HCT564	CD74HC/HCT564	Octal D Flip-Flop, Three-State, Inverting	20	1640
CD54HC/HCT573	CD74HC/HCT573	Octal Transparent Latch, Three-State	20	1679
CD54HC/HCT574	CD74HC/HCT574	Octal D Flip-Flop, Three-State	20	1663
CD54HC/HCT583	CD74HC/HCT583	4-Bit BCD Full Adder with Fast Carry	16	1828
CD54HC/HCT597	CD74HC/HCT597	8-Bit Shift Register with Input Storage	16	1915
CD54HC/HCT640	CD74HC/HCT640	Octal Bus Transceiver, Three-State, Inverting	20	1677
CD54HC/HCT643	CD74HC/HCT643	Octal Bus Transceiver, Three-State, True/Inverting	20	1677
CD54HC/HCT646	CD74HC/HCT646	Octal Bus Transceiver/Register, Three-State	24	1664
CD54HC/HCT648	CD74HC/HCT648	Octal Bus Transceiver/Register, Three-State, Inverting	24	1664
CD54HC/HCT651	CD74HC/HCT651	Octal Bus Transceiver/Register, Three-State, Inverting	24	2229
CD54HC/HCT652	CD74HC/HCT652	Octal Bus Transceiver/Register, Three-State, Non-Inverting	24	2229
CD54HC/HCT670	CD74HC/HCT670	4 x 4 Register File, Three-State	16	1660
CD54HC/HCT688	CD74HC/HCT688	8-Bit Magnitude Comparator	20	1646
CD54HC/HCT4002	CD74HC/HCT4002	Dual 4-Input NOR Gate	14	1776
CD54HC/HCT4015	CD74HC/HCT4015	Dual 4-Stage Static Shift Register	16	1678
CD54HC/HCT4016	CD74HC/HCT4016	Quad Bilateral Switch	14	1917
CD54HC/HCT4017	CD74HC/HCT4017	Decade Counter/Divider with 10 Decoded Outputs	16	1639
CD54HC/HCT4020	CD74HC/HCT4020	14-Stage Binary Ripple Counter	16	1484
CD54HC/HCT4024	CD74HC/HCT4024	7-Stage Binary Ripple Counter	14	1683
CD54HC/HCT4040	CD74HC/HCT4040	12-Bit Binary Counter	16	1483
CD54HC/HCT4046A	CD74HC/HCT4046A	Phase-Locked Loop with VCO	16	1854
CD54HC4049	CD74HC4049	Hex Inverting High-to-Low Level Shifter	16	1543
CD54HC4050	CD74HC4050	Hex High-to-Low Level Shifter	16	1543
CD54HC/HCT4051	CD74HC/HCT4051	8-Channel Analog Multiplexer/Demultiplexer	16	1676
CD54HC/HCT4052	CD74HC/HCT4052	Dual 4-Channel Analog Multiplexer/Demultiplexer	16	1676
CD54HC/HCT4053	CD74HC/HCT4053	Triple 2-Channel Analog Multiplexer/Demultiplexer	16	1676
CD54HC/HCT4059	CD74HC/HCT4059	Programmable Divide by "N" Counter	24	1853
CD54HC/HCT4060	CD74HC/HCT4060	14-Stage Binary Counter with Oscillator	16	1654
CD54HC/HCT4066	CD74HC/HCT4066	Quad Bilateral Switch	14	1777
CD54HC/HCT4067	CD74HC/HCT4067	16-Channel Analog Multiplexer/Demultiplexer	24	1783
CD54HC/HCT4075	CD74HC/HCT4075	Triple 3-Input OR Gate	14	1778
CD54HC/HCT4094	CD74HC/HCT4094	8-Stage Shift-and-Store Bus Register	16	1779
CD54HC/HCT4316	CD74HC/HCT4316	Quad Analog Switch	16	1916

HC/HCT Series Data Sheet AnswerFAX Document Listing (Continued)

смоѕ	LOGIC	DESCRIPTION	NUMBER OF LEADS	ANSWERFAX DOCUMENT NUMBER
CD54HC/HCT4353	CD74HC/HCT4353	Analog MUX with Latch	20	2145
CD54HC/HCT4510	CD74HC/HCT4510	Up/Down Counter, BCD	16	1823
CD54HC/HCT4511	CD74HC/HCT4511	BCD-to-7-Segment Latch/Decoder/Driver	16	1786
CD54HC/HCT4514	CD74HC/HCT4514	4-to-16-Line Decoder/Demultiplexer with Input Latch	24	1597
CD54HC/HCT4515	CD74HC/HCT4515	4-to-16-Line Decoder with Input Latches	24	1597
CD54HC/HCT4516	CD74HC/HCT4516	Up/Down Counter, Binary	16	1823
CD54HC/HCT4518	CD74HC/HCT4518	Dual Synchronous BCD Counter	16	1665
CD54HC/HCT4520	CD74HC/HCT4520	Dual 4-Bit Synchronous Binary Counter	16	1665
CD54HC/HCT4538	CD74HC/HCT4538	Dual Precision Monostable Multivibrator	16	1671
CD54HC/HCT4543	CD74HC/HCT4543	BCD-to-7-Segment Latch Decoder/Driver for LCDs	16	1822
CD54HC/HCT7030	CD74HC/HCT7030	9-Bit x 64 Word FIFO Register, Three-State	28	2122
CD54HC/HCT7046	CD74HC/HCT7046	Phase-Locked Loop with In-Lock Detection	16	1917
CD54HC7266	CD74HC7266	Quad EXCLUSIVE-NOR Gate	14	1780
CD54HC/HCT40102	CD74HC/HCT40102	8-Bit Synchronous BCD Down Counter	16	1596
CD54HC/HCT40103	CD74HC/HCT40103	8-Bit Binary Down Counter	16	1596
CD54HC/HCT40104	CD74HC/HCT40104	4-Bit Bidirectional Universal Shift Register, Three-State	16	1661
CD54HC/HCT40105	CD74HC/HCT40105	4 Bits x 16 Words FIFO Register	16	1834
CD54HCU04	CD74HCU04	Hex Inverter (Unbuffered)	14	1655

AC/ACT Series Data Sheet AnswerFAX Document Listing

СМО	S LOGIC	DESCRIPTION	NUMBER OF LEADS	ANSWERFAX DOCUMENT NUMBER
CD54AC/ACT00	CD74AC/ACT00	Quad 2-Input NAND Gate	14	1855
CD54AC/ACT02	CD74AC/ACT02	Quad 2-Input NOR Gate	14	1978
CD54AC/ACT04	CD74AC/ACT04	Hex Inverter/Buffer	14	1945
CD54AC/ACT05	CD74AC/ACT05	Hex Inverter/Buffer with Open-Drain Outputs	14	1945
CD54AC/ACT08	CD74AC/ACT08	Quad 2-Input AND Gate	14	1950
CD54AC/ACT10	CD74AC/ACT10	Triple 3-Input NAND Gate	14	1977
CD54AC/ACT14	CD74AC/ACT14	Hex Inverting Schmitt Trigger	14	1984
CD54AC/ACT20	CD74AC/ACT20	Dual 4-Input NAND Gate	14	1976
CD54AC/ACT32	CD74AC/ACT32	Quad 2-Input OR Gate	14	1951
CD54AC/ACT74	CD74AC/ACT74	Dual D Flip-Flop with Set and Reset	14	1881
CD54AC/ACT86	CD74AC/ACT86	Quad 2-Input Exclusive-OR Gate	14	1952
CD54AC/ACT109	CD74AC/ACT109	Dual J-K Flip-Flop with Set and Reset	16	1967
CD54AC/ACT112	CD74AC/ACT112	Dual J-K Flip-Flop with Set and Reset	16	1967
CD54AC/ACT138	CD74AC/ACT138	3-to-8-Line Decoder/Demultiplexer, Inverting	16	1909
CD54AC/ACT139	CD74AC/ACT139	Dual 2-to-4-Line Decoder/Demultiplexer	16	1953
CD54AC/ACT151	CD74AC/ACT151	8-Input Multiplexer	16	1980
CD54AC/ACT153	CD74AC/ACT153	Dual 4-Input Multiplexer	16	1966
CD54AC/ACT157	CD74AC/ACT157	Quad 2-Input Multiplexer	16	1910
CD54AC/ACT158	CD74AC/ACT158	Quad 2-Input Multiplexer, Inverting	16	1910

AC/ACT Series Data Sheet AnswerFAX Document Listing (Continued)

СМО	S LOGIC	DESCRIPTION	NUMBER OF LEADS	ANSWERFA) DOCUMENT NUMBER
CD54AC/ACT161	CD74AC/ACT161	Synchronous 4-Bit Binary Counter, Asynchronous Reset	16	1959
CD54AC/ACT163	CD74AC/ACT163	Synchronous 4-Bit Binary Counter, Synchronous Reset	16	1959
CD54AC/ACT164	CD74AC/ACT164	8-Bit Serial-In/Parallel-Out Shift Register	14	1954
CD54AC/ACT174	CD74AC/ACT174	Hex D-Type Flip-Flop with Reset	16	1973
CD54AC/ACT175	CD74AC/ACT175	Quad D-Type Flip-Flop with Reset	16	1964
CD54AC/ACT191	CD74AC/ACT191	Synchronous 4-Bit Binary Up/Down Counter	16	1911
CD54AC/ACT193	CD74AC/ACT193	Synchronous 4-Bit Binary Up/Down Counter	16	1947
CD54AC/ACT238	CD74AC/ACT238	3-to-8-Line Decoder/Demultiplexer	16	1909
CD54AC/ACT240	CD74AC/ACT240	Octal Buffer/Line Driver, Three-State, Inverting	20	1856
CD54AC/ACT241	CD74AC/ACT241	Octal Buffer/Line Driver, Three-State	20	1856
CD54AC/ACT244	CD74AC/ACT244	Octal-Buffer/Line Driver, Three-State	20	1856
CD54AC/ACT245	CD74AC/ACT245	Octal-Bus Transceiver, Three-State	20	1907
CD54AC/ACT251	CD74AC/ACT251	8-Input Multiplexer, Three-State	16	1981
CD54AC/ACT253	CD74AC/ACT253	Dual 4-Input Multiplexer, Three-State	16	1985
CD54AC/ACT257	CD74AC/ACT257	Quad 2-Input Multiplexer, Three-State	16	1955
CD54AC/ACT258	CD74AC/ACT258	Quad 2-Input Multiplexer, Three-State	16	1955
CD54AC/ACT273	CD74AC/ACT273	Octal D-Type Flip-Flop with Reset	20	1979
CD54AC/ACT280	CD74AC/ACT280	8-Bit Odd/Even Parity Generator/Checker	14	1957
CD54AC/ACT283	CD74AC/ACT283	4-Bit Full Adder with Fast Carry	16	1912
CD54AC/ACT297	CD74AC/ACT297	Digital Phase-Locked Loop	16	2195
CD54AC/ACT299	CD74AC/ACT299	8-Bit Universal Shift Register, Three-State	20	1958
CD54AC/ACT323	CD74AC/ACT323	8-Bit Universal Shift Register, Three-State, (with Synchronous Reset)	20	1958
CD54AC/ACT373	CD74AC/ACT373	Octal Transparent Latch, Three-State	20	1882
CD54AC/ACT374	CD74AC/ACT374	Octal D Flip-Flop, Three-State	20	1883
CD54AC/ACT533	CD74AC/ACT533	Octal Transparent Latch, Three-State, Inverting	20	1882
CD54AC/ACT534	CD74AC/ACT534	Octal D Flip-Flop, Three-State, Inverting	20	1883
CD54AC/ACT540	CD74AC/ACT540	Octal Buffer/Line Driver, Three-State, Inverting	20	1857
CD54AC/ACT541	CD74AC/ACT541	Octal Buffer/Line Driver, Three-State	20	1857
CD54AC/ACT563	CD74AC/ACT563	Octal Inverting Transparent Latch, Three-State	20	1956
CD54AC/ACT564	CD74AC/ACT564	Octal D-Type Flip-Flop, Three-State, Inverting	20	1948
CD54AC/ACT573	CD74AC/ACT573	Octal Transparent Latch, Three-State	20	1949
CD54AC/ACT574	CD74AC/ACT574	Octal D-Type Flip-Flop, Three-State	20	1948
CD54AC/ACT623	CD74AC/ACT623	Octal-Bus Transceiver, Three-State, Non-Inverting	20	1968
CD54AC/ACT646	CD74AC/ACT646	Octal-Bus Transceiver/Register, Three-State	24	1970
CD54AC/ACT647	CD74AC/ACT647	Octal-Bus Transceiver/Register with Open Drain, Non-Inverting	24	1982
CD54AC/ACT648	CD74AC/ACT648	Octal Bus Transceiver/Register, Three-State, Inverting	24	1970
CD54AC/ACT651	CD74AC/ACT651	Octal-Bus Transceiver/Register, Three-State, Inverting	24	1974
CD54AC/ACT652	CD74AC/ACT652	Octal-Bus, Transceiver/Register, Three-State, Non-Inverting	24	1974
CD54AC/ACT653	CD74AC/ACT653	Octal-Bus Transceiver/Register; Open-Drain (A-Side); Three-State (B Side); Inverting	24	1975

AC/ACT Series Data Sheet AnswerFAX Document Listing (Continued)

смоѕ	LOGIC	DESCRIPTION	NUMBER OF LEADS	ANSWERFAX DOCUMENT NUMBER
CD54AC/ACT654	CD74AC/ACT654	Octal-Bus Transceiver/Register; Open-Drain (A-Side); Three-State (B Side); Non-Inverting	24	1975
CD54AC/ACT7060	CD74AC/ACT7060	14-Stage Binary Counter with Oscillator	20	2062
CD54AC/ACT7623	CD74AC/ACT7623	Octal-Bus Transceiver/Register; Open-Drain (A-Side); Three-State (B Side); Non-Inverting	20	1969

FCT Series Data Sheet AnswerFAX Document Listing

смоѕ	LOGIC	DESCRIPTION	NUMBER OF LEADS	ANSWERFAX DOCUMENT NUMBER
CD54FCT240	CD74FCT240	Octal Buffer/Line Driver, Three-State, Inverting	20	2227
CD54FCT241	CD74FCT241	Octal Buffer/Line Driver, Three-State	20	2227
CD54FCT244	CD74FCT244	Octal Buffer/Line Driver, Three-State	20	2227
CD54FCT245	CD74FCT245	Octal-Bus Transceiver, Three-State	20	2301
CD54FCT273	CD74FCT273	Octal D Flip-Flop with Reset	20	2303
CD54FCT373	CD74FCT373	Octal Transparent Latch, Three-State	20	2230
CD54FCT374	CD74FCT374	Octal D-Type Flip-Flop, Three-State	20	2305
CD54FCT533	CD74FCT533	Octal Transparent Latch, Three-State, Inverting	20	2230
CD54FCT540	CD74FCT540	Octal Buffer/Line Driver, Three-State, Inverting	20	2383
CD54FCT541	CD74FCT541	Octal Buffer/Line Driver, Three-State	20	2383
CD54FCT543	CD74FCT543	Octal Register/Transceiver, Three-State	24	2399
CD54FCT564	CD74FCT564	Octal D-Type Flip-Flop, Three-State, Inverting	20	2295
CD54FCT573	CD74FCT573	Octal Transparent Latch, Three-State	20	2304
CD54FCT574	CD74FCT574	Octal D-Type Flip-Flop, Three-State	20	2295
CD54FCT623	CD74FCT623	Octal Bus Transceiver, Three-State	20	2302
CD54FCT646	CD74FCT646	Octal Bus Transceiver/Register, Three-State	24	2393
CD54FCT651	CD74FCT641	Octal Bus Transceiver/Register, Three-State, Inverting	24	2394
CD54FCT652	CD74FCT652	Octal Bus Transceiver/Register, Three-State	24	2394
CD54FCT653	CD74FCT653	Octal Bus Transceiver/Register, Open-Drain (A Side), Three-State (B Side), Inverting	24	2403
CD54FCT654	CD74FCT654	Octal Bus Transceiver/Register, Open-Drain (A Side), Three-State (B Side)	24	2403
CD54FCT821A	CD74FCT821A	10-Bit D-Type Flip-Flop, Three-State	24	2390
CD54FCT822A	CD74FCT822A	10-Bit D-Type Flip-Flop, Three-State, Inverting	24	2390
CD54FCT823A	CD74FCT823A	9-Bit D-Type Flip-Flop, Three-State	24	2389
CD54FCT824A	CD74FCT824A	9-Bit D-Type Flip-Flop, Three-State, Inverting	24	2389
CD54FCT841A	CD74FCT841A	10-Bit Transparent Latch, Three-State	24	2397
CD54FCT842A	CD74FCT842A	10-Bit Transparent Latch, Three-State, Inverting	24	2397
CD54FCT843A	CD74FCT843A	9-Bit Transparent Latch, Three-State	24	2396
CD54FCT844A	CD74FCT844A	9-Bit Transparent Latch, Three-State, Inverting	24	2396
CD54FCT861A	CD74FCT861A	10-Bit Bus Transceiver, Three-State	24	2392
CD54FCT863A	CD74FCT863A	9-Bit Bus Transceiver, Three-State	24	2391
CD54FCT2952A	CD74FCT2952A	Octal Register/Transceiver, Three-State	24	2400
CD54FCT7623	CD74FCT7623	Octal Bus Transceiver, Three-State (B Side), Open-Drain (A Side)	20	2358

CD4000 Series Data Sheet AnswerFAX Document Listing

CMOS LOGIC	DESCRIPTION	NUMBER OF LEADS	ANSWERFAX DOCUMENT NUMBER
CD4001B	CMOS NOR Gate	14	985
CD4001UB	CMOS Quad 2-Input NOR Gate	14	945
CD4002B	CMOS NOR Gate	14	985
CD4006B	CMOS 18-Stage Static Shift Register	14	1033
CD4007UB	CMOS Dual Complementary Pair Plus Inverter	14	977
CD4008B	CMOS 4-Bit Full Adder	16	951
CD4009UB	CMOS Hex Buffer/Converter	16	940
CD4010B	CMOS Hex Buffer/Converter	16	940
CD4011B	CMOS NAND Gate	14	3718
CD4011UB	CMOS Quad 2-Input NAND Gate	14	947
CD4012B	CMOS NAND Gate	14	3718
CD4013B	CMOS Dual D-Type Flip-Flop	14	936
CD4014B	CMOS 8-Stage Static Shift Register	16	1043
CD4015B	CMOS Dual 4-Stage Static Shift Register	16	1024
CD4016B	CMOS Quad Bilateral Switch	14	953
CD4017B	CMOS Counter/Divider	16	1113
CD4018B	CMOS Presettable Divide-By-N Counter	16	1034
CD4019B	CMOS Quad AND/OR Select Gate	16	1045
CD4020B	CMOS Ripple-Carry Binary Counter/Divider (14 Stage)	16	1063
CD4021B	CMOS 8-Stage Static Shift Register	16	1043
CD4022B	CMOS Counter/Divider	16	1113
CD4023B	CMOS NAND Gate	14	3718
CD4024B	CMOS Ripple-Carry Binary Counter/Divider (7 Stage)	14	1063
CD4025B	CMOS NOR Gate	14	985
CD4026B	CMOS Decade Counter/Divider	16	1118
CD4027B	CMOS Dual J-K Master-Slave Flip-Flop	16	942
CD4028B	CMOS BCD-to-Decimal Decoder	16	1016
CD4029B	CMOS Presettable Up/Down Counter	16	1028
CD4030B	CMOS Quad Exclusive-OR Gate	14	1055
CD4031B	CMOS 64-Stage Static Shift Register	16	1073
CD4033B	CMOS Decade Counter/Divider	16	1118
CD4034B	CMOS 8-Stage Static Bidirectional Parallel/Serial Input/Output Bus Register	24	1062
CD4035B	CMOS 4-Stage Parallel-In/Parallel-Out Shift Register	16	1101
CD4040B	CMOS Ripple-Carry Binary Counter/Divider (12 Stage)	16	1063
CD4041UB	CMOS Quad True/Complement Buffer	14	934

CD4000 Series Data Sheet AnswerFAX Document Listing (Continued)

CMOS LOGIC	DESCRIPTION	NUMBER OF LEADS	ANSWERFAX DOCUMENT NUMBER
CD4042B	CMOS Quad Clocked D Latch	16	954
CD4043B	CMOS Quad Three-State R/S Latch	16	956
CD4044B	CMOS Quad Three-State R/S Latch	16	956
CD4045B	CMOS 21-Stage Counter	16	1119
CD4046B	CMOS Micropower Phase-Locked Loop	16	1099
CD4047B	CMOS Low-Power Monostable/Astable Multivibrator	14	1123
CD4048B	CMOS Multifunction Expandable 8-Input Gate	16	1124
CD4049UB	CMOS Hex Buffer/Converter	16	926
CD4050B	CMOS Hex Buffer/Converter	16	926
CD4051B	CMOS Analog Multiplexer/Demultiplexer	16	902
CD4052B	CMOS Analog Multiplexer/Demultiplexer	16	902
CD4053B	CMOS Analog Multiplexer/Demultiplexer	16	902
CD4054B	CMOS Liquid-Crystal Display Driver	16	634
CD4055B	CMOS Liquid-Crystal Display Driver	16	634
CD4056B	CMOS Liquid-Crystal Display Driver	16	634
CD4059A	CMOS Programmable Divide-By-N Counter	24	898
CD4060B	CMOS 14-Stage Ripple-Carry Binary Counter/Divider and Oscillator	16	1120
CD4063B	CMOS 4-Bit Magnitude Comparator	16	805
CD4066B	CMOS Quad Bilateral Switch	14	1114
CD4067B	CMOS Analog Multiplexer/Demultiplexer	24	3719
CD4068B	CMOS 8-Input NAND/AND Gate	14	809
CD4069UB	CMOS Hex Inverter	14	804
CD4070B	CMOS Quad Exclusive-OR Gate	14	910
CD4071B	CMOS OR Gate	14	807
CD4072B	CMOS OR Gate	14	807
CD4073B	CMOS AND Gate	14	806
CD4075B	CMOS OR Gate	14	807
CD4076B	CMOS 4-Bit D-Type Register	16	903
CD4077B	CMOS Quad Exclusive-NOR Gate	14	910
CD4078B	CMOS 8-Input NOR/OR Gate	14	810
CD4081B	CMOS AND Gate	14	806
CD4082B	CMOS AND Gate	14	806
CD4085B	CMOS Dual 2-Wide AND-OR-INVERT Gate	14	811
CD4086B	CMOS Expandable 4-Wide 2-Input AND-OR-INVERT Gate	14	812
CD4089B	CMOS Binary Rate Multiplier	16	1003

CD4000 Series Data Sheet AnswerFAX Document Listing (Continued)

CMOS LOGIC	DESCRIPTION	NUMBER OF LEADS	ANSWERFA) DOCUMENT NUMBER
CD4093B	CMOS Quad 2-Input NAND Schmitt Trigger	14	836
CD4094B	CMOS 8-Stage Shift-and-Store Bus Register	16	3707
CD4095B	CMOS Gated J-K Master-Slave Flip-Flop	14	879
CD4096B	CMOS Gated J-K Master-Slave Flip-Flop	14	879
CD4097B	CMOS Analog Multiplexer/Demultiplexer	24	3719
CD4098B	CMOS Dual Monostable Multivibrator	16	979
CD4099B	CMOS 8-Bit Addressable Latch	16	948
CD4502B	CMOS Strobed Hex Inverter/Buffer	16	1002
CD4503B	CMOS Hex Buffer	16	1224
CD4504B	CMOS Hex Voltage-Level Shifter for TTL-to-CMOS or CMOS-to-CMOS Operation	16	1846
CD4508B	CMOS Dual 4-Bit Latch	24	1009
CD4510B	CMOS Presettable Up/Down Counter	16	899
CD4511B	CMOS BCD-to-7-Segment Latch Decoder Driver	16	901
CD4512B	CMOS 8-Channel Data Selector	16	1032
CD4514B	CMOS 4-Bit Latch/4-to-16-Line Decoder	24	3721
CD4515B	CMOS 4-Bit Latch/4-to-16-Line Decoder	24	3721
CD4516B	CMOS Presettable Up/Down Counter	16	899
CD4517B	CMOS Dual 64-Stage Static Shift Register	16	1148
CD4518B	CMOS Dual Up Counter	16	808
CD4519B	CMOS 4-Bit AND/OR Selector, Quad 2-Channel Data Selector, or Quad Exclusive NOR Gate	16	1723
CD4520B	CMOS Dual Up Counter	16	808
CD4521B	CMOS 24-Stage Frequency Divider	16	1735
CD4522B	CMOS Programmable BCD Divide-By-N Counter	16	1710
CD4527B	CMOS BCD Rate Multiplier	16	1006
CD4529B	CMOS Dual 4-Channel Analog Data Selector	16	1720
CD4532B	CMOS 8-Bit Priority Encoder	16	876
CD4536B	CMOS Programmable Timer	16	1186
CD4541B	CMOS Programmable Timer	. 14	1378
CD4543B	CMOS BCD-to-7-Segment Latch/Decoder/Driver for Liquid-Crystal Display	16	1327
CD4555B	CMOS Dual Binary-to-1-to-4 Decoder/Demultiplexer	16	858
CD4556B	CMOS Dual Binary-to-1-to-4 Decoder/Demultiplexer	16	858
CD4560B	CMOS NBCD Adder	16	1711
CD4566B	CMOS Industrial Time-Based Generator	16	1728
CD4572UB	CMOS Hex Gate	16	1704
CD4585B	CMOS 4-Bit Magnitude Comparator	16	1146

CD4000 Series Data Sheet AnswerFAX Document Listing (Continued)

CMOS LOGIC	DESCRIPTION	NUMBER OF LEADS	ANSWERFAX DOCUMENT NUMBER
CD4724B	CMOS 8-Bit Addressable Latch	16	1111
CD7211	CMOS 4-Digit LCD Decoder/Driver	40	1725
CD7211A	CMOS 4-Digit LCD Decoder/Driver	40	1725
CD7211AM	CMOS 4-Digit LCD Decoder/Driver	40	1726
CD7211M	CMOS 4-Digit LCD Decoder/Driver	40	1726
CD14538B	CMOS Dual Precision Monostable Multivibrator	16	3737
CD22402	CMOS LSI Sync Generator	24	1686
CD22777	CMOS 32kHz Quartz Analog Clock Circuit	8	1869
CD40100B	CMOS 32-Stage Static Left/Right Shift Register	16	980
CD40102B	CMOS 8-Stage Presettable Synchronous Down Counter	16	984
CD40103B	CMOS 8-Stage Presettable Synchronous Down Counter	16	984
CD40105B	CMOS FIFO Register	16	1044
CD40106B	CMOS Hex Schmitt Trigger	14	1017
CD40107B	CMOS Dual 2-Input NAND Buffer/Driver	8, 14	1015
CD40109B	CMOS Quad Low-to-High Voltage Level Shifter	16	3722
CD40110B	CMOS Decade Up-Down Counter/Latch/Display Driver	16	1125
CD40116	CMOS High Speed 8-Bit Bidirectional CMOS/TTL Interfaced Level Converter	22	1234
CD40117B	Programmable Dual 4-Bit Terminator	14	1333
CD40147B	10-Line to 4-Line BCD Priority Encoder	16	1117
CD40160B	CMOS Synchronous Programmable 4-Bit Counter	16	1047
CD40161B	CMOS Synchronous Programmable 4-Bit Counter	16	1047
CD40163B	CMOS Synchronous Programmable 4-Bit Counter	16	1047
CD40174B	CMOS Hex D-Type Flip-Flop	16	1031
CD40175B	CMOS Quad D-Type Flip-Flop	16	1326
CD40192B	CMOS Presettable Up/Down Counter (Dual Clock with Reset)	16	993
CD40193B	CMOS Presettable Up/Down Counter (Dual Clock with Reset)	16	993
CD40194B	CMOS 4-Bit Bidirectional Universal Shift Register	16	1220
CD40257B	CMOS Quad 2-Line-to-1-Line Data Selector/Multiplexer	16	982

Harris CMOS Logic Families

High Speed CMOS (HC/HCT) Logic SSI, MSI Logic Functions and Low Current Bus Interface Devices

Features

- 3µm CMOS Process
- · HCT Provides Drop-In Replacement for LSTTL
- · HC Provides Direct Interface to CMOS
- Typical Gate Propagation Delay = 8ns at 5V
- · JEDEC Standard 4mA, 6mA Sink/Source Drive Current Capability
- · 2V to 6V Operation for HC Devices
- 4.5V to 5.5V Operation for HCT Devices

Advanced CMOS (AC/ACT) Logic SSI, MSI Logic Functions and Medium Current Bus Interface Devices

Features

- 1.5μm CMOS Process
- · ACT Provides Drop-In Replacement for Bipolar FAST
- · AC Provides Direct Interface to CMOS
- Typical Gate Propagation Delay = 3ns at 5V
- JEDEC Standard 24mA Sink/Source Drive Current Capability
- 1.5V to 5.5V Operation for AC Devices
- · 4.5V to 5.5V Operation for ACT Devices
- Low Groundbounce V_{OLP} = 1V Typical

FCT Bus Interface Devices

Features

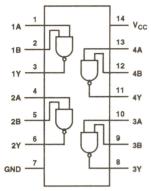
- · 8-Bit, 9-Bit, and 10-Bit High Current Drive Bus Interface Devices
- 1.5μm, Low Power BiCMOS Process
- Drop-In Replacement for Bipolar FAST and AS Logic
- Typical Gate Propagation Delay = 3ns at 5V
- JEDEC Standard 64mA, 48mA Sink Current Capability
- 4.75V to 5.25V Operation
- No Input/Output Diodes to V_{CC}
 - Eliminates Bus Contention
 - Allows Hot Card Insertion
- Low Groundbounce V_{OLP} = 1V Typical

CD4000 Logic SSI and MSI Logic Functions

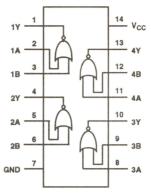
Features

- 7µm CMOS Process
- · CMOS Input Compatibility
- Typical Gate Propagation Delay = 60ns at 5V
- JEDEC Standard 0.4mA Sink/Source Drive Current Capability
- · High Voltage Operation
 - 3V to 18V Operation for B Series
 - 3V to 12V Operation for A Series
- · High Noise Immunity at 10V to 15V; Ideal for Noisy Environments

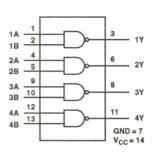
HC/HCT CMOS Logic Functional Diagrams



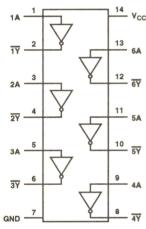
QUAD 2-INPUT NAND GATE CD54/74HC00, CD54/74HCT00



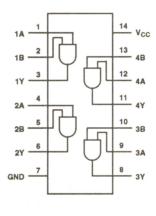
QUAD 2-INPUT NOR GATE CD54/74HC02, CD54/74HCT02



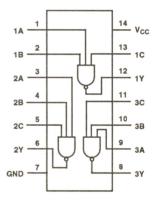
QUAD 2-INPUT NAND GATE WITH OPEN DRAIN CD54/74HC03, CD54/74HCT03



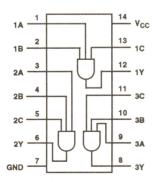
HEX INVERTER
CD54/74HC04, CD54/74HCT04



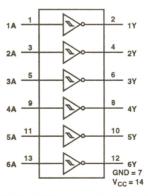
QUAD 2-INPUT AND GATE CD54/74HC08, CD54/74HC108



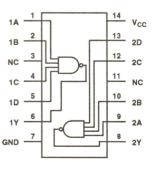
TRIPLE 3-INPUT NAND GATE CD54/74HC10, CD54/74HC110



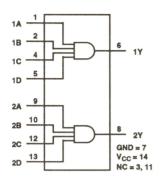
TRIPLE 3-INPUT AND GATE CD54/74HC11, CD54/74HC111



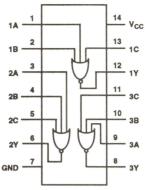
HEX INVERTING SCHMITT TRIGGER
CD54/74HC14, CD54/74HCT14



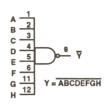
DUAL 4-INPUT NAND GATE CD54/74HC20, CD54/74HCT20



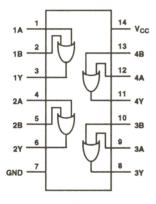
DUAL 4-INPUT AND GATE CD54/74HC21, CD54/74HCT21



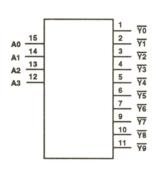
TRIPLE 3-INPUT NOR GATE CD54/74HC27, CD54/74HCT27



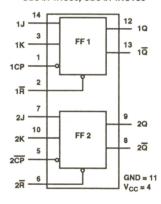
8-INPUT NAND GATE CD54/74HC30, CD54/74HCT30



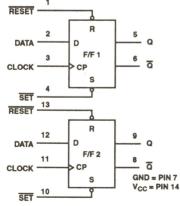
QUAD 2-INPUT OR GATE CD54/74HC32, CD54/74HC32



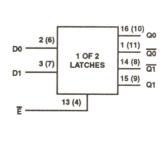
BCD-TO-DECIMAL DECODER (1-OF-10) CD54/74HC42, CD54/74HCT42



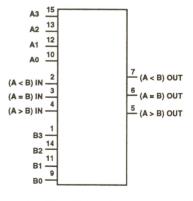
DUAL J-K FLIP-FLOP WITH RESET, NEGATIVE-EDGE TRIGGER CD54/74HC73, CD54/74HC73



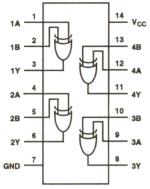
DUAL D FLIP-FLOP WITH SET AND RESET, POSITIVE-EDGE TRIGGER CD54/74HC74, CD54/74HC774



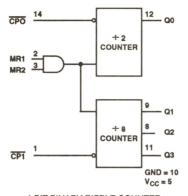
DUAL 2-BIT BISTABLE TRANSPARENT LATCH CD54/74HC75, CD54/74HCT75



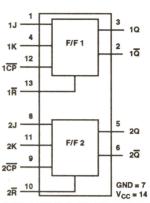
4-BIT MAGNITUDE COMPARATOR CD54/74HC85, CD54/74HCT85



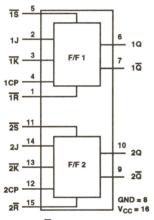
QUAD 2-INPUT EXCLUSIVE-OR GATE CD54/74HC86, CD54/74HC786



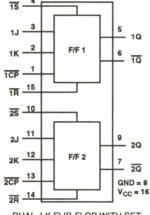
4-BIT BINARY RIPPLE COUNTER CD54/74HC93, CD54/74HCT93



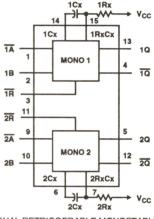
DUAL J-K FLIP-FLOP WITH RESET, NEGATIVE-EDGE TRIGGER CD54/74HC107, CD54/74HCT107



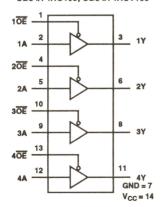
DUAL J-K FLIP-FLOP WITH SET AND RESET CD54/74HC109. CD54/74HCT109



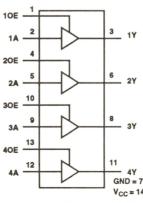
DUAL J-K FLIP-FLOP WITH SET AND RESET CD54/74HC112. CD54/74HCT112



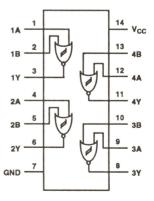
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET CD54/74HC123/423, CD54/74HCT123/423



QUAD BUFFER, THREE-STATE CD54/74HC125, CD54/74HC1125

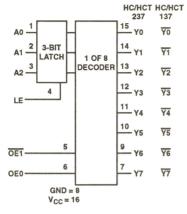


QUAD BUFFER, THREE-STATE CD54/74HC126, CD54/74HC126

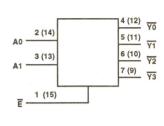


QUAD 2-INPUT NAND SCHMITT TRIGGER CD54/74HC132, CD54/74HC132

HC/HCT CMOS Logic Functional Diagrams (Continued)

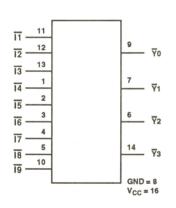


нс/нст нс/нст 15 YO ٧n A0 14 VI 13 3 <u>Y2</u> A2 -12 V3 11 Y4 <u>V4</u> 10 Y5 ET -**Y5** 9 5 <u>76</u> E2 -7 77 E3 -

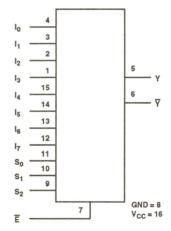


3-TO-8-LINE DECODER/
DEMULTIPLEXER,
WITH ADDRESS LATCHES
INVERTING AND NON-INVERTING
CD54/74HC137/237, CD54/74HC1137/237

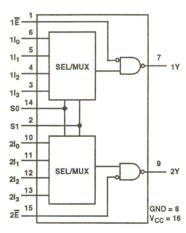
3-TO-8-LINE DECODER/ DEMULTIPLEXER, INVERTING AND NON-INVERTING CD54/74HC138/238, CD54/74HC1138/238 DUAL 2-TO-4 LINE DECODER/ DEMULTIPLEXER CD54/74HC139, CD54/74HC1139



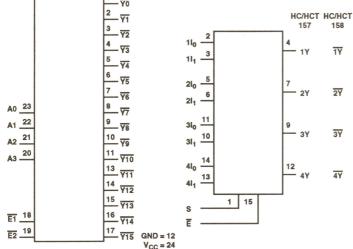
10-TO-4-LINE PRIORITY ENCODER CD54/74HC147, CD54/74HCT147



8-INPUT MULTIPLEXER CD54/74HC151, CD54/74HC151



DUAL 4-INPUT MULTIPLEXER CD54/74HC153, CD54/74HC153



P0 P1 P2 P3

3 4 5 6

SPE 9

CP 2

MR 1

PE 7

TE 10

TE 10

TE 10

TE 10

TE 17

TE 17

TE 17

TE 18

TE 1

4-TO-16-LINE DECODER/DEMULTIPLEXER CD54/74HC154, CD54/74HCT154

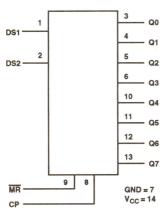
QUAD 2-INPUT MULTIPLEXER, NON-INVERTING CD54/74HC/HCT157

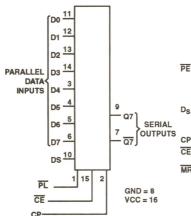
QUAD 2-INPUT MULTIPLEXER, INVERTING CD54/74HC/HCT158 PRESETTABLE COUNTERS, BCD DECADE COUNTER, ASYNCHRONOUS RESET CD54/74HC/HCT160

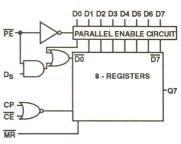
PRESETTABLE COUNTERS, 4-BIT BINARY COUNTER, ASYNCHRONOUS RESET CD54/74HC/HCT161

PRESETTABLE COUNTERS, BCD DECADE COUNTER, SYNCHRONOUS RESET CD54/74HC/HCT162

PRESETTABLE COUNTERS, 4-BIT BINARY COUNTER, SYNCHRONOUS RESET CD54/74HC/HCT163

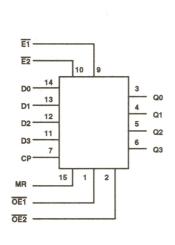


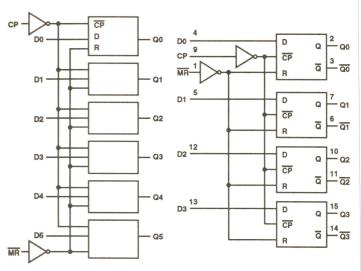




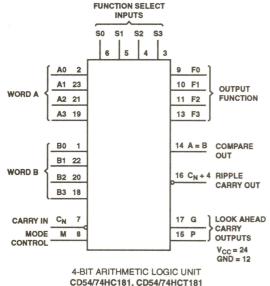
8-BIT SERIAL-IN/PARALLEL-OUT SHIFT REGISTER CD54/74HC164, CD54/74HCT164 8-BIT PARALLEL-IN/SERIAL-OUT SHIFT REGISTER CD54/74HC165, CD54/74HCT165 8-BIT PARALLEL-IN/SERIAL-OUT SHIFT REGISTER CD54/74HC166, CD54/74HCT166

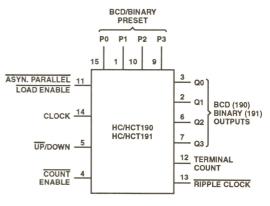
HC/HCT CMOS Logic Functional Diagrams (Continued)





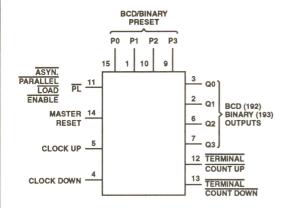
QUAD D-TYPE FLIP-FLOP, THREE-STATE, POSITIVE-EDGE TRIGGERED CD54/74HC173, CD54/74HCT173 HEX D-TYPE FLIP-FLOP WITH RESET, POSITIVE-EDGE TRIGGERED CD54/74HC174, CD54/74HC1174 QUAD D FLIP-FLOP WITH RESET CD54/74HC175, CD54/74HC175





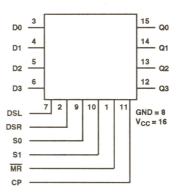
PRESETTABLE SYNCHRONOUS 4-BIT UP/DOWN
BCD DECADE COUNTER
CD54/74HC/HCT190

PRESETTABLE SYNCHRONOUS 4-BIT UP/DOWN
BINARY COUNTER
CD54/74HC/HCT191

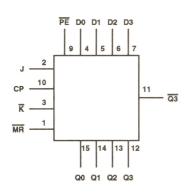


PRESETTABLE SYNCHRONOUS 4-BIT UP/DOWN BCD DECADE COUNTER, ASYNCHRONOUS RESET CD54/74HC/HCT192

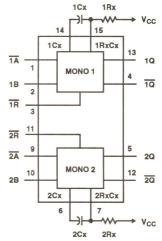
PRESETTABLE SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTER, ASYNCHRONOUS RESET CD54/74HC/HCT193



4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER CD54/74HC194, CD54/74HCT194



4-BIT PARALLEL ACCESS REGISTER CD54/74HC195, CD54/74HCT195

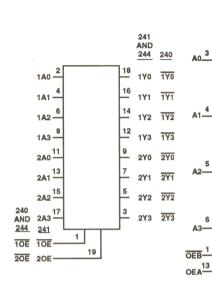


DUAL MONOSTABLE MULTIVIBRATOR WITH RESET CD54/74HC221, CD54/74HCT221

11_{B0}

ΔO

HC/HCT CMOS Logic Functional Diagrams (Continued)



QUAD-BUS TRANSCEIVER WITH THREE-STATE OUTPUTS, INVERTING CD54/74HC242, CD54/74HCT242

DIRECTION

SELECT LOGIC

A1 4 10 B1

A2 5 9 B2

A3 6 8 B3

OEB 13 DIRECTION SELECT LOGIC

QUAD-BUS TRANSCEIVER WITH

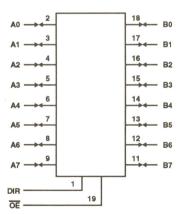
R0

QUAD-BUS TRANSCEIVER WITH THREE-STATE OUTPUTS, NON-INVERTING CD54/74HC243, CD54/74HCT243

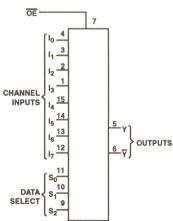
OCTAL BUFFER/LINE DRIVERS, THREE-STATE, INVERTING CD54/74HC/HCT240

OCTAL BUFFER/LINE DRIVERS, THREE-STATE, NON-INVERTING CD54/74HC/HCT241

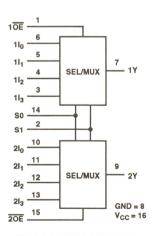
OCTAL BUFFER/LINE DRIVERS, THREE-STATE, NON-INVERTING CD54/74HC/HCT244



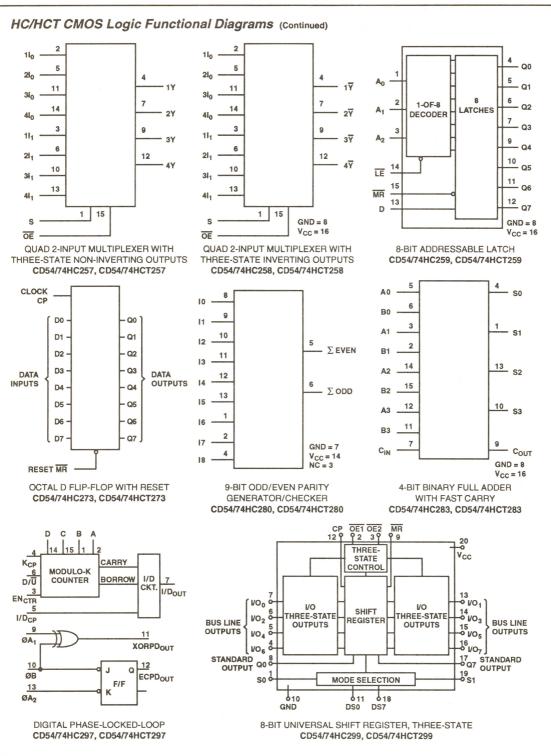
OCTAL-BUS TRANSCEIVER, THREE-STATE, NON-INVERTING CD54/74HC245, CD54/74HCT245

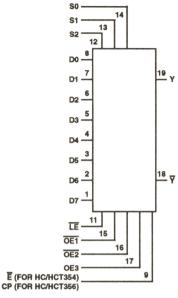


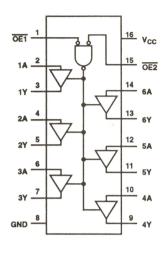
8-INPUT MULTIPLEXER, THREE-STATE CD54/74HC251, CD54/74HC251

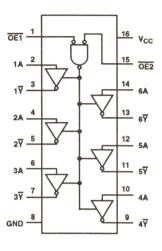


DUAL 4-INPUT MULTIPLEXER CD54/74HC253, CD54/74HCT253





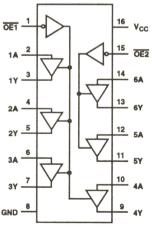




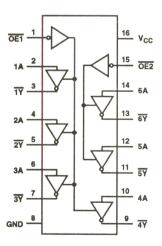
8-INPUT MULTIPLEXER/REGISTER, THREE-STATE, TRANSPARENT DATA AND SELECT LATCHES CD54/74HC/HCT354

8-INPUT MULTIPLEXER/REGISTER, THREE-STATE, EDGE-TRIGGERED DATA FLIP-FLOPS AND TRANSPARENT SELECT LATCHES CD54/74HC/HCT356 HEX BUFFER/LINE DRIVER, THREE-STATE, NON-INVERTING CD54/74HC365, CD54/74HCT365

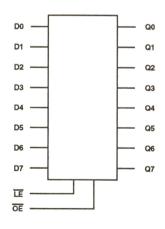
HEX BUFFER/LINE DRIVER, THREE-STATE, INVERTING CD54/74HC366, CD54/74HCT366



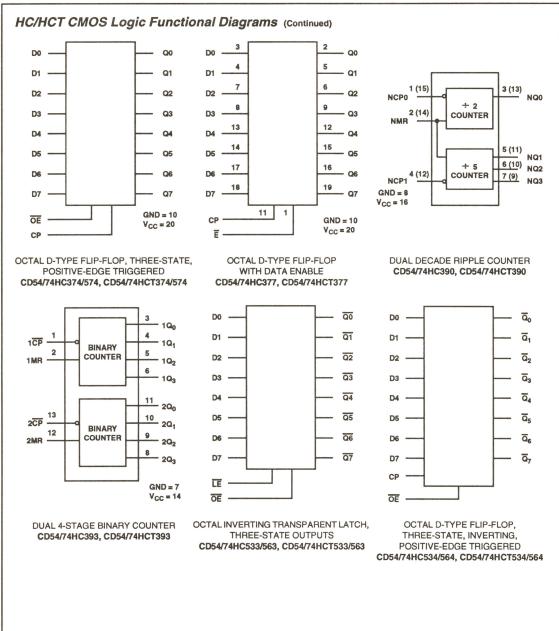
HEX BUFFER/LINE DRIVER, THREE-STATE, NON-INVERTING CD54/74HC367, CD54/74HCT367

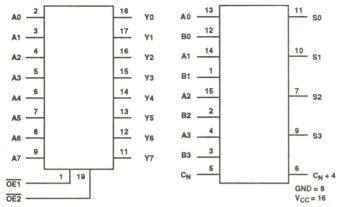


HEX BUFFER/LINE DRIVER, THREE-STATE, INVERTING CD54/74HC368, CD54/74HCT368

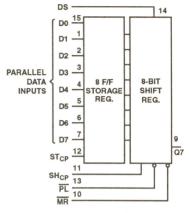


OCTAL TRANSPARENT LATCH, THREE-STATE OUTPUT CD54/74HC373/573, CD54/74HCT373/573

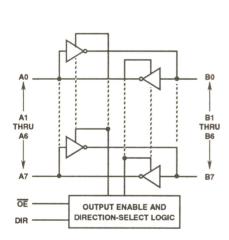




OCTAL BUFFER AND LINE DRIVER, THREE-STATE CD54/74HC540/541, CD54/74HCT540/541 4-BIT BCD FULL ADDER WITH FAST CARRY CD54/74HC583, CD54/74HCT583

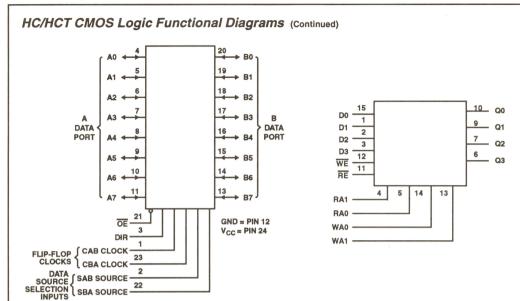


8-BIT SHIFT REGISTER WITH INPUT STORAGE CD54/74HC597, CD54/74HCT597



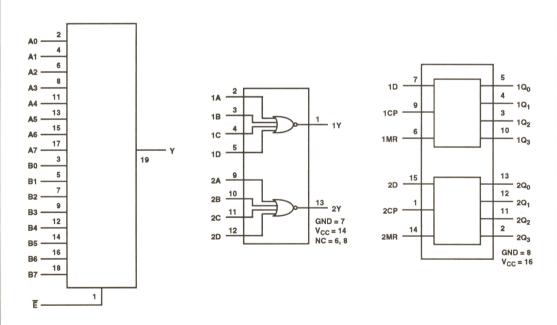
OCTAL THREE-STATE BUS TRANSCEIVER, INVERTING CD54/74HC640, CD54/74HCT640

OCTAL THREE-STATE BUS TRANSCEIVER, TRUE/INVERTING CD54/74HC643, CD54/74HC7643



OCTAL BUS TRANSCEIVER/REGISTER, THREE-STATE CD54/74HC646/648, CD54/74HCT646/648

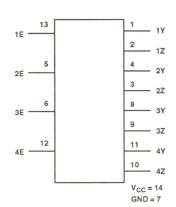
4 X 4 REGISTER FILE CD54/74HC670, CD54/74HCT670

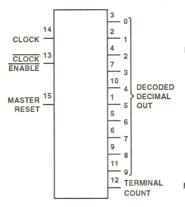


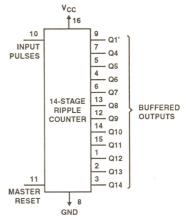
8-BIT MAGNITUDE COMPARATOR CD54/74HC688, CD54/74HCT688

DUAL 4-INPUT NOR GATE
CD54/74HC4002, CD54/74HCT4002

DUAL 4-STAGE STATIC SHIFT REGISTER CD54/74HC4015, CD54/74HCT4015



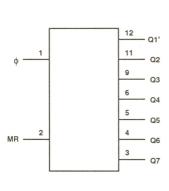


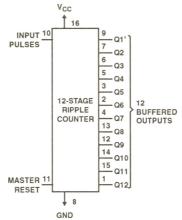


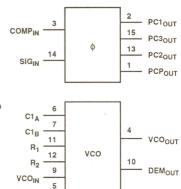
QUAD BILATERAL SWITCH CD54/74HC4016, CD54/74HCT4016

DECADE COUNTER/DIVIDER
WITH 10 DECODED OUTPUTS
CD54/74HC4017, CD54/74HCT4017

14-STAGE BINARY COUNTER CD54/74HC4020, CD54/74HCT4020



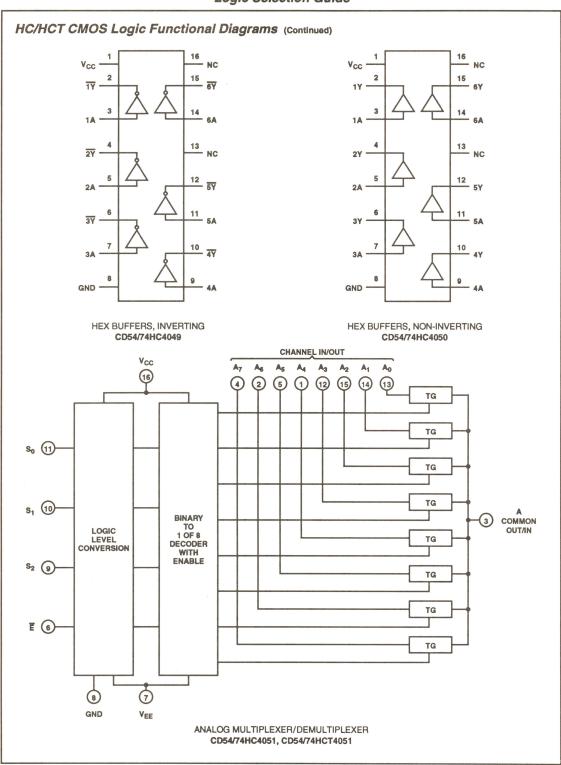


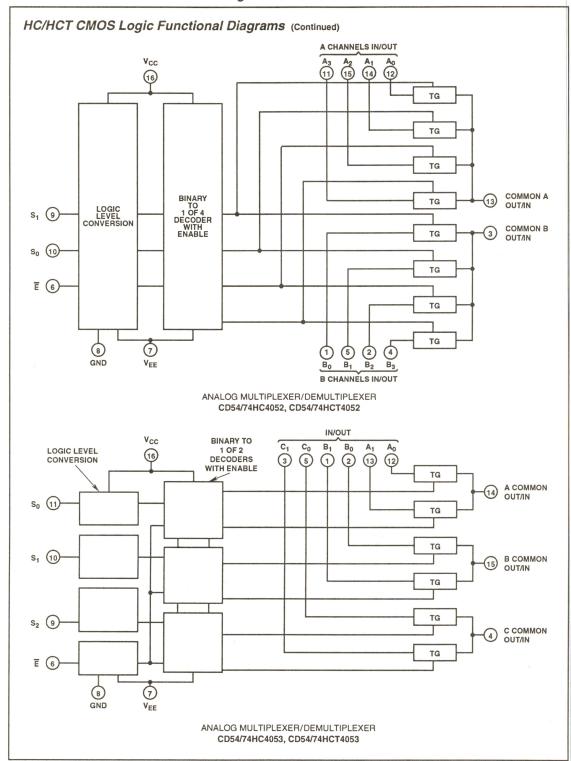


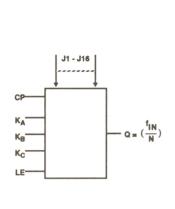
7-STAGE BINARY RIPPLE COUNTER CD54/74HC4024, CD54/74HCT4024

12-STAGE BINARY COUNTER CD54/74HC4040. CD54/74HCT4040

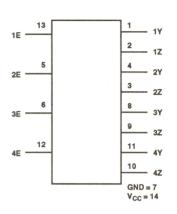
PHASE-LOCKED-LOOP WITH VCO
CD54/74HC4046A, CD54/74HCT4046A







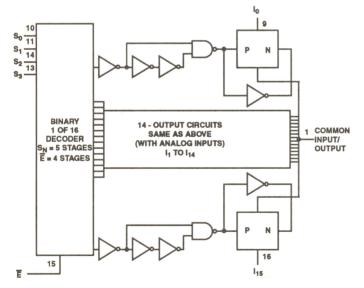
5 4 12 6 14-STAGE RIPPLE 14 COUNTER 13 11 AND Q9 OSCILLATOR 15 1 Q12 2 013 3 Q14 фΟ GND = 8 10 V_{CC} = 16 φ0

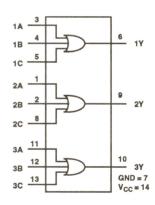


CMOS PROGRAMMABLE DIVIDE-BY -"N" COUNTER CD54/74HC4059, CD54/74HCT4059

14-STAGE BINARY COUNTER WITH OSCILLATOR CD54/74HC4060, CD54/74HCT4060

QUAD BILATERAL SWITCH CD54/74HC4066, CD54/74HCT4066

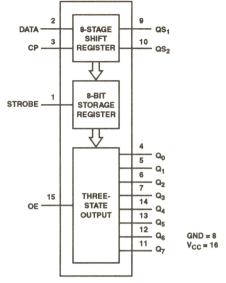


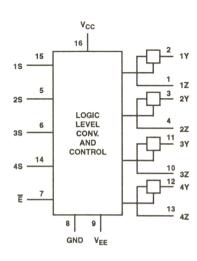


16-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER CD54/74HC4067, CD54/74HCT4067

TRIPLE 3-INPUT OR GATE CD54/74HC4075, CD54/74HCT4075

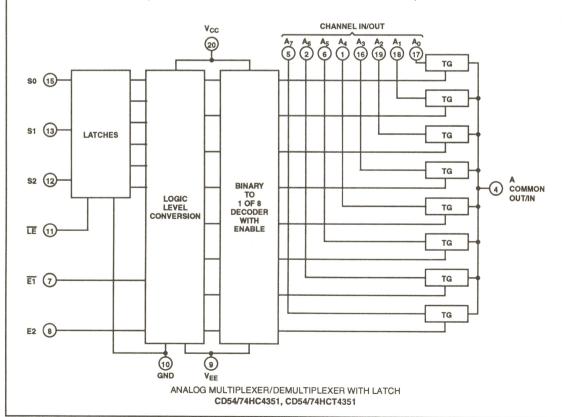


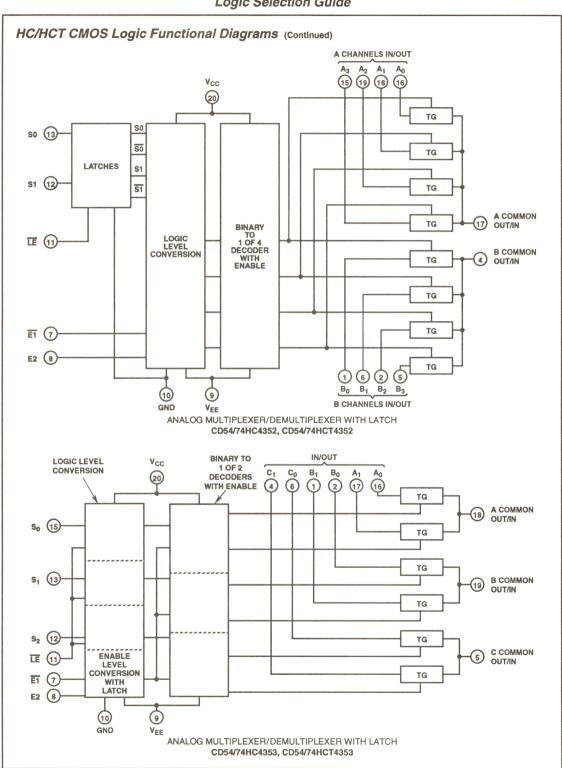


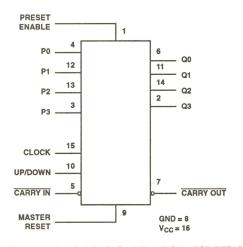


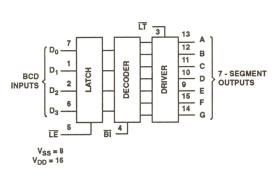
8-STAGE SHIFT-AND-STORE BUS REGISTER, THREE-STATE CD54/74HC4094, CD54/74HCT4094

QUAD ANALOG SWITCH WITH LEVEL TRANSLATION CD54/74HC4316, CD54/74HCT4316





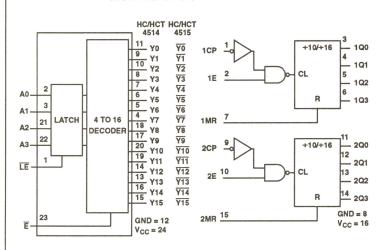


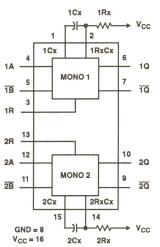


PRESETTABLE SYNCHRONOUS 4-BIT UP/DOWN BCD DECADE COUNTER, ASYNCHRONOUS RESET CD54/74HC/HCT4510

BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER CD54/74HC4511, CD54/74HCT4511

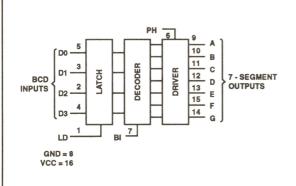
PRESETTABLE SYNCHRONOUS 4-BIT UP/DOWN BINARY
COUNTER, ASYNCHRONOUS RESET
CD54/74HC/HCT4516

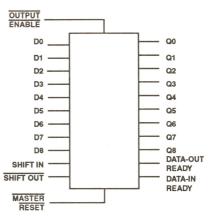




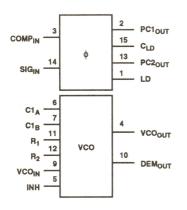
4-TO-16 LINE DECODER/
DEMULTIPLEXER WITH INPUT LATCH
CD54/74HC4514/4515,
CD54/74HCT4514/4515

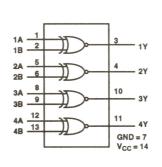
DUAL SYNCHRONOUS COUNTER, BCD CD54/74HC/HCT4518 DUAL SYNCHRONOUS COUNTER, BINARY DUAL RETRIGGERABLE PRECISION MONOSTABLE MULTIVIBRATOR CD54/74HC4538, CD54/74HCT4538

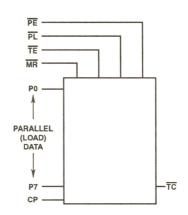




BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER FOR LCDs CD54/74HC4543, CD54/74HCT4543 64-WORD X 9-BIT FIFO REGISTER, THREE-STATE CD54/74HC7030, CD54/74HCT7030





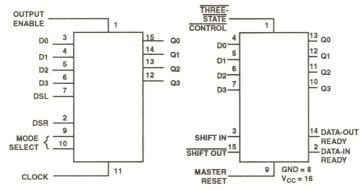


PHASE-LOCKED LOOP WITH VCO AND LOCK DETECTOR CD54/74HC7046A, CD54/74HCT7046A

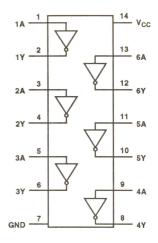
QUAD 2-INPUT EXCLUSIVE-NOR GATE CD54/74HC7266

8-STAGE SYNCHRONOUS DOWN COUNTER, 2-DECADE BCD TYPE CD54/74HC/HCT40102

8-STAGE SYNCHRONOUS DOWN COUNTER, 8-BIT BINARY TYPE CD54/74HC/HCT40103

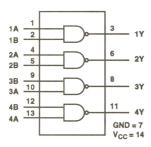


4-BIT UNIVERSAL BIDIRECTIONAL SHIFT REGISTER CD54/74HC40104, CD54/74HCT40104 4-BIT X 16-WORD FIFO REGISTER
CD54/74HC40105, CD54/74HCT40105

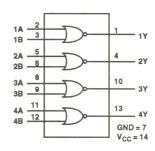


HEX INVERTER CD54/74HCU04

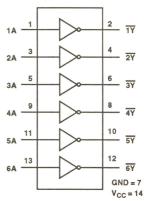
AC/ACT CMOS Logic Functional Diagrams



QUAD 2-INPUT NAND GATE CD54/74AC00, CD54/74ACT00

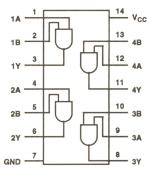


QUAD 2-INPUT NOR GATE CD54/74AC02, CD54/74ACT02

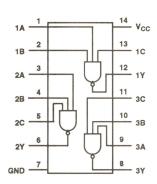


HEX INVERTERS, ACTIVE OUTPUTS CD54/74AC/ACT04

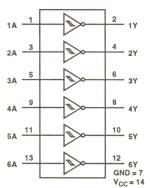
HEX INVERTERS, OPEN-DRAIN OUTPUTS CD54/74AC/ACT05



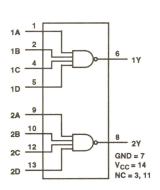
QUAD 2-INPUT AND GATE CD54/74AC08, CD54/74ACT08



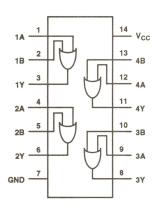
TRIPLE 3-INPUT NAND GATE CD54/74AC10, CD54/74AC110



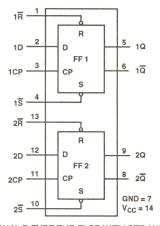
HEX INVERTING SCHMITT TRIGGER CD54/74AC14, CD54/74ACT14



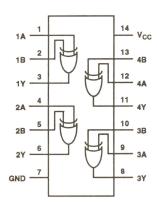
DUAL 4-INPUT NAND GATE CD54/74AC20, CD54/74ACT20



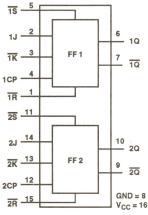
QUAD 2-INPUT OR GATE CD54/74AC32, CD54/74ACT32



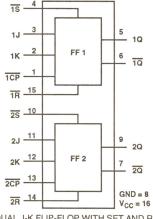
DUAL D-TYPE FLIP-FLOP WITH SET AND RESET, POSITIVE-EDGE TRIGGERED CD54/74AC74, CD54/74AC774



QUAD 2-INPUT EXCLUSIVE-OR GATE CD54/74AC86, CD54/74AC86

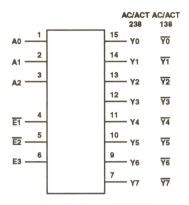


DUAL J-K FLIP-FLOP WITH SET AND RE-SET, POSITIVE-EDGE TRIGGERED (J, K) CD54/74AC109, CD54/74ACT109



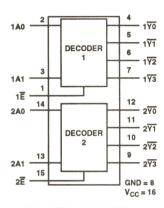
DUAL J-K FLIP-FLOP WITH SET AND RE-SET, NEGATIVE-EDGE TRIGGERED (J, K) CD54/74AC112, CD54/74ACT112

AC/ACT CMOS Logic Functional Diagrams (Continued)

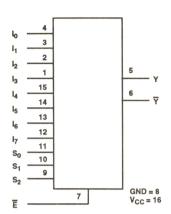


3-TO-8-LINE DECODER/ DEMULTIPLEXERS, INVERTING CD54/74AC/ACT138

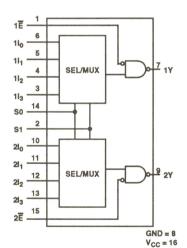
3-TO-8-LINE DECODER/
DEMULTIPLEXERS, NON-INVERTING
CD54/74AC/ACT238



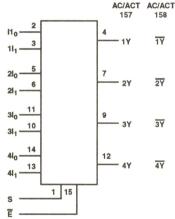
DUAL 2-TO-4-LINE DECODER/ DEMULTIPLEXER CD54/74AC139, CD54/74AC139



8-INPUT MULTIPLEXER CD54/74AC151, CD54/74AC151

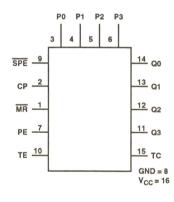


DUAL 4-INPUT MULTIPLEXER CD54/74AC153, CD54/74AC153



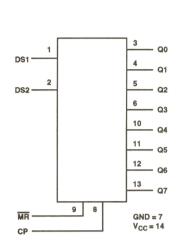
QUAD 2-INPUT MULTIPLEXER, NON-INVERTING CD54/74AC/ACT157

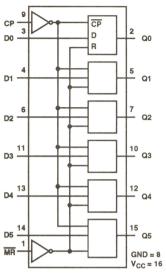
QUAD 2-INPUT MULTIPLEXER, INVERTING CD54/74AC/ACT158

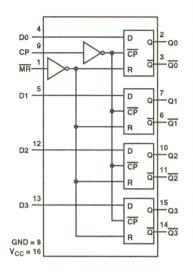


SYNCHRONOUS PRESETTABLE BINARY COUNTER, ASYNCHRONOUS RESET CD54/74AC/ACT161

SYNCHRONOUS PRESETTABLE BINARY COUNTER, SYNCHRONOUS RESET CD54/74AC/ACT163



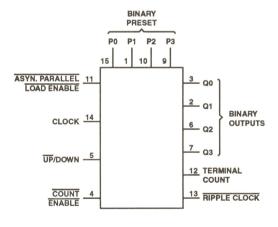


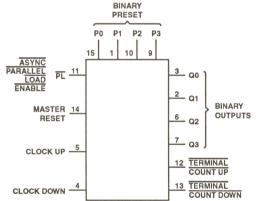


8-BIT SERIAL-IN/PARALLEL-OUT SHIFT REGISTER CD54/74AC164, CD54/74ACT164

HEX D FLIP-FLOP WITH RESET CD54/74AC174, CD54/74AC174

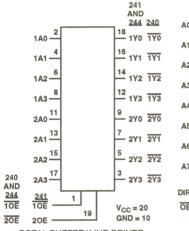
QUAD D FLIP-FLOP WITH RESET CD54/74AC175, CD54/74AC175





PRESETTABLE SYNCHRONOUS 4-BIT BINARY UP/DOWN CONVERTER CD54/74AC191, CD54/74ACT191

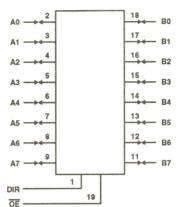
PRESETTABLE SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER WITH RESET CD54/74AC193, CD54/74ACT193



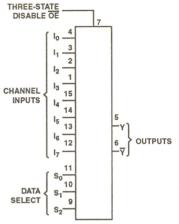
OCTAL BUFFER/LINE DRIVER, THREE-STATE, INVERTING CD54/74AC/ACT240

OCTAL BUFFER/LINE DRIVER, THREE-STATE, NON-INVERTING CD54/74AC/ACT241

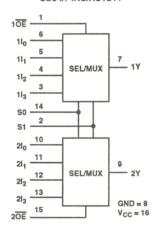
OCTAL BUFFER/LINE DRIVER, THREE-STATE, NON-INVERTING CD54/74AC/ACT244



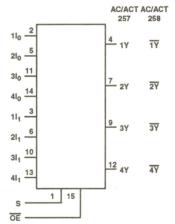
OCTAL-BUS TRANSCEIVER, THREE-STATE, NON-INVERTING CD54/74AC245, CD54/74ACT245



8-INPUT MULTIPLEXER, THREE-STATE CD54/74AC251, CD54/74ACT251

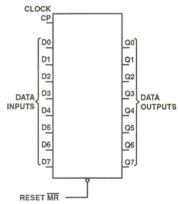


DUAL 4-INPUT MULTIPLEXER, THREE-STATE CD54/74AC253, CD54/74ACT253

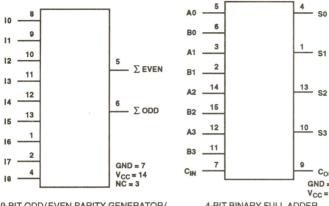


QUAD 2-INPUT MULTIPLEXER WITH THREE-STATE, NON-INVERTING OUTPUTS CD54/74AC/ACT257

QUAD 2-INPUT MULTIPLEXER WITH THREE-STATE, INVERTING OUTPUTS CD54/74AC/ACT258



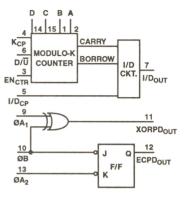
OCTAL D FLIP-FLOP WITH RESET CD54/74AC273, CD54/74ACT273



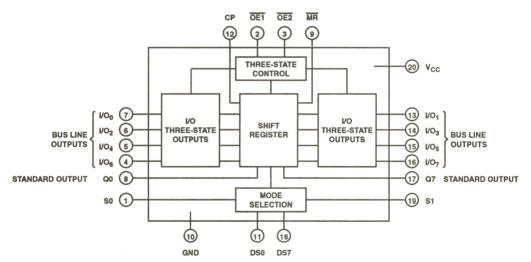
9-BIT ODD/EVEN PARITY GENERATOR/ CHECKER CD54/74AC280, CD54/74ACT280

COUT GND = 8 V_{CC} = 16 4-BIT BINARY FULL ADDER

WITH FAST CARRY CD54/74AC283, CD54/74ACT283

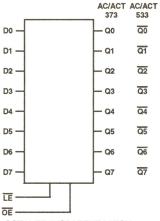


DIGITAL PHASE-LOCKED LOOP CD54/74AC297, CD54/74ACT297



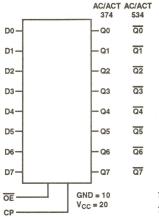
8-INPUT UNIVERSAL SHIFT/STORAGE REGISTER WITH COMMON PARALLEL I/O PINS, ASYNCHRONOUS RESET CD54/74AC/ACT299

8-INPUT UNIVERSAL SHIFT/STORAGE REGISTER WITH COMMON PARALLEL I/O PINS, SYNCHRONOUS RESET CD54/74AC/ACT323



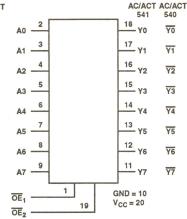
OCTAL TRANSPARENT LATCH, THREE-STATE, NON-INVERTING CD54/74AC/ACT373

OCTAL TRANSPARENT LATCH, THREE-STATE, INVERTING CD54/74AC/ACT533



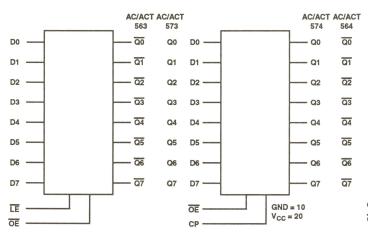
OCTAL D-TYPE FLIP-FLOPS, THREE-STATE, POSITIVE-EDGE TRIGGERED, NON-INVERTING CD54/74AC/ACT374

OCTAL D-TYPE FLIP-FLOPS, THREE-STATE, POSITIVE-EDGE TRIGGERED, INVERTING CD54/74AC/ACT534



OCTAL BUFFER/LINE DRIVERS, THREE-STATE, INVERTING CD54/74AC/ACT540

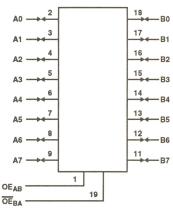
OCTAL BUFFER/LINE DRIVERS, THREE-STATE, NON-INVERTING CD54/74AC/ACT541



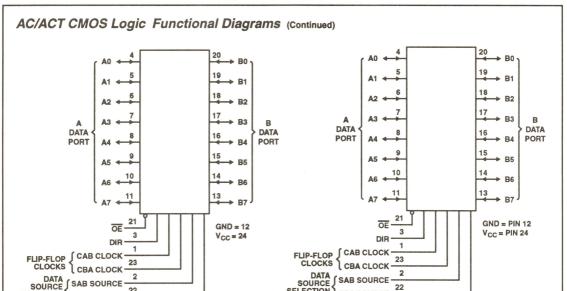
OCTAL TRANSPARENT LATCH, THREE-STATE, INVERTING CD54/74AC/ACT563

OCTAL TRANSPARENT LATCH, THREE-STATE, NON-INVERTING CD54/74AC/ACT573 OCTAL D-TYPE FLIP-FLOP, THREE-STATE, POSITIVE-EDGE TRIGGERED, INVERTING CD54/74AC/ACT564

OCTAL D-TYPE FLIP-FLOP, THREE-STATE, POSITIVE-EDGE-TRIGGERED, NON-INVERTING CD54/74AC/ACT574



OCTAL-BUS TRANSCEIVER, THREE-STATE, NON-INVERTING CD54/74AC623, CD54/74ACT623



OCTAL-BUS TRANSCEIVER/REGISTER, THREE-STATE, NON-INVERTING CD54/74AC/ACT646

SAB SOURCE

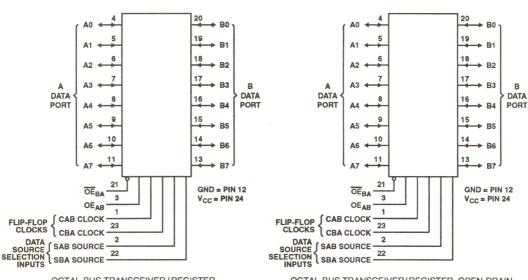
SELECTION SBA SOURCE

OCTAL-BUS TRANSCEIVER/REGISTER, THREE-STATE, INVERTING CD54/74AC/ACT648

OCTAL-BUS TRANSCEIVER/REGISTER, WITH OPEN DRAIN, NON-INVERTING CD54/74AC647, CD54/74ACT647

SAB SOURCE

SELECTION SBA SOURCE



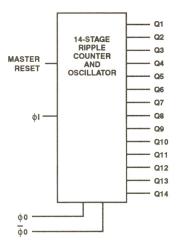
OCTAL-BUS TRANSCEIVER/REGISTER, THREE-STATE, INVERTING CD54/74AC/ACT651

OCTAL-BUS TRANSCEIVER/REGISTER, THREE-STATE, NON-INVERTING CD54/74AC/ACT652

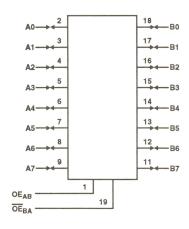
OCTAL-BUS TRANSCEIVER/REGISTER, OPEN-DRAIN (A SIDE), THREE-STATE (B SIDE), INVERTING CD54/74AC/ACT653

OCTAL-BUS TRANSCEIVER/REGISTER, OPEN-DRAIN (A SIDE), THREE-STATE (B SIDE), NON-INVERTING CD54/74AC/ACT654

AC/ACT CMOS Logic Functional Diagrams (Continued)

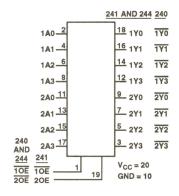


14-STAGE BINARY COUNTER WITH OSCILLATOR CD54/74AC7060, CD54/74ACT7060



OCTAL-BUS TRANSCEIVER, THREE-STATE (B SIDE), OPEN-DRAIN (A SIDE), NON-INVERTING CD54/74AC7623, CD54/74ACT7623

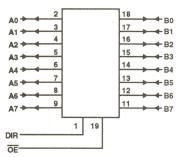
FCT CMOS Logic Functional Diagrams



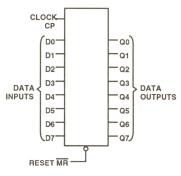
OCTAL BUFFERS/LINE DRIVER, THREE-STATE, INVERTING CD54/74FCT240/240AT

OCTAL BUFFERS/LINE DRIVER, THREE-STATE, NON-INVERTING CD54/74FCT241

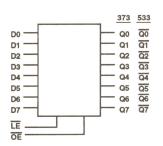
OCTAL BUFFERS/LINE DRIVER, THREE-STATE, NON-INVERTING CD54/74FCT244/244AT



OCTAL-BUS TRANSCEIVER, THREE-STATE, NON-INVERTING CD54/74FCT245, CD54/74FCT245AT



OCTAL D FLIP-FLOP WITH RESET CD54/74FCT273



D0 00 D1 Q1 Q2 D2 D3 Q3 D4 ΩA D5 Q5 D6 Q6 D7 **Q7** $V_{CC} = 20$ ŌĒ GND = 10 CP

541 540 18 2 A0 ΥO 3 17 <u>Y1</u> 16 <u>Y2</u> A2 15 **Y3** 14 ¥4 A4 13 **Y**5 A5 12 **Y6** A6 11 **Y7** $V_{CC} = 20$ OE1 GND = 10 OE2

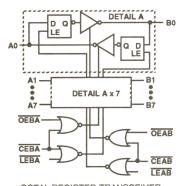
OCTAL TRANSPARENT LATCH, THREE-STATE, NON-INVERTING CD54/74FCT373/373AT

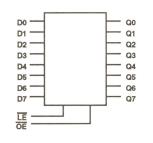
OCTAL D-TYPE FLIP-FLOP. THREE-STATE, POSITIVE-EDGE TRIGGER. **NON-INVERTING** CD54/74FCT374, CD54/74FCT374AT

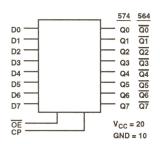
OCTAL BUFFERS/LINE DRIVER. THREE-STATE, INVERTING CD54/74FCT540

OCTAL TRANSPARENT LATCH. THREE-STATE, INVERTING CD54/74FCT533

OCTAL BUFFER/LINE DRIVER. THREE-STATE, NON-INVERTING CD54/74FCT541



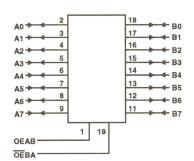


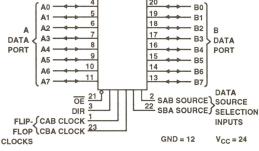


OCTAL REGISTER-TRANSCEIVER, THREE-STATE, NON-INVERTING CD54/74FCT543

OCTAL TRANSPARENT LATCH, THREE-STATE, NON-INVERTING CD54/74FCT573, CD54/74FCT573AT OCTAL D-TYPE FLIP-FLOP, THREE-STATE, POSITIVE-EDGE TRIGGERED, INVERTING CD54/74FCT564

OCTAL D-TYPE FLIP-FLOP, THREE-STATE, POSITIVE-EDGE TRIGGERED. NON-INVERTING CD54/74FCT574, CD54/74FCT574AT





OCTAL-BUS TRANSCEIVER, THREE-STATE, NON-INVERTING CD54/74FCT623

OCTAL BUS TRANSCEIVER/REGISTER, THREE-STATE, NON-INVERTING CD54/74FCT646, CD54/74FCT646AT

A0

A1

A2

A3

A5

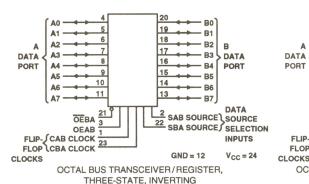
AG

Δ7

FLIP- CAB CLOCK

Α

FCT CMOS Logic Functional Diagrams (Continued)



OCTAL BUS TRANSCEIVER/REGISTER, OPEN-DRAIN (A SIDE), THREE-STATE (B-SIDE), INVERTING CD54/74FCT653

5

6

7

8

9

10

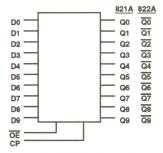
11

OEBA

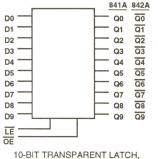
OEAB

CD54/74FCT651 OCTAL BUS TRANSCEIVER/REGISTER, THREE-STATE, NON-INVERTING CD54/74FCT652

OCTAL BUS TRANSCEIVER/REGISTER, OPEN-DRAIN (A SIDE), THREE-STATE (B-SIDE), NON-INVERTING CD54/74FCT654



823A 824A QO QO D₀ D1 Q1 Q1 Q2 D2 Q2 Q3 D3 03 Q4 **D4** Q4 Q5 Q5 **D5** D6 Q6 Q6 Q7 **D7** Q7 Da OR CE CP OE MR



B0

B1

B2 В

B3

B4 PORT

B5

B6

R7

SAB SOURCE \SOURCE

GND = 12

SBA SOURCE SELECTION

DATA

DATA

INPUTS

 $V_{CC} = 24$

19

18

16

15

10-BIT D-TYPE FLIP-FLOP, THREE-STATE, POSITIVE-EDGE TRIGGERED, NON-INVERTING CD54/74FCT821A

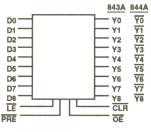
9-BIT D-TYPE FLIP-FLOP, THREE-STATE. POSITIVE-EDGE TRIGGERED. NON-INVERTING CD54/74FCT823A

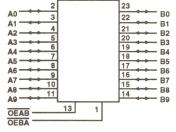
THREE-STATE, NON-INVERTING CD54/74FCT841A

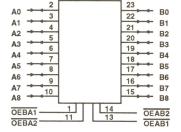
10-BIT D-TYPE FLIP-FLOP, THREE-STATE, POSITIVE-EDGE TRIGGERED, INVERTING CD54/74FCT822A

9-BIT D-TYPE FLIP-FLOP, THREE-STATE, POSITIVE-EDGE TRIGGERED, INVERTING CD54/74FCT824A

10-BIT TRANSPARENT LATCH. THREE-STATE, INVERTING CD54/74FCT842A





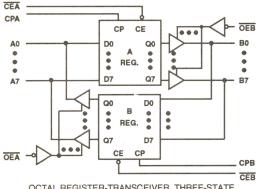


9-BIT TRANSPARENT LATCH, THREE-STATE, NON-INVERTING CD54/74FCT843A

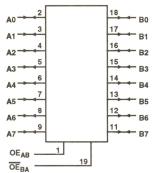
10-BIT BUS TRANSCEIVER, THREE-STATE, NON-INVERTING CD54/74FCT861A

9-BIT BUS TRANSCEIVER, THREE-STATE, NON-INVERTING CD54/74FCT863A

9-BIT TRANSPARENT LATCH. THREE-STATE, INVERTING CD54/74FCT844A

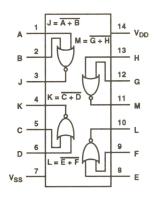


OCTAL REGISTER-TRANSCEIVER, THREE-STATE,
NON-INVERTING
CD54/74FCT2952A

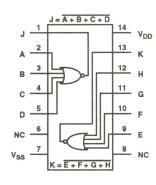


OCTAL BUS TRANSCEIVER, THREE-STATE (B SIDE), OPEN-DRAIN (A SIDE), NON-INVERTING CD54/74FCT7623

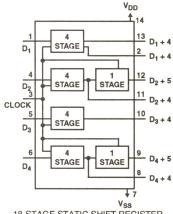
CD4000 CMOS Logic Functional Diagrams



QUAD 2-INPUT NOR GATE CD4001B, CD4001UB

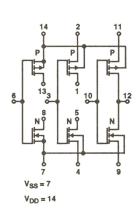


DUAL 4-INPUT NOR GATE CD4002B

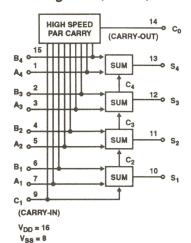


18-STAGE STATIC SHIFT REGISTER CD4006B

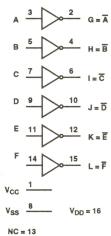
CD4000 CMOS Logic Functional Diagrams (Continued)



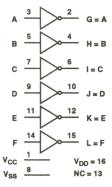
DUAL COMPLEMENTARY PAIR
PLUS INVERTER
CD4007UB



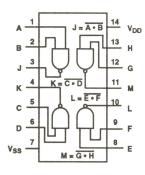
4-BIT FULL ADDER WITH PARALLEL CARRY OUT CD4008B



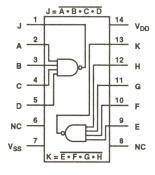
HEX BUFFER/CONVERTER, INVERTING TYPE CD4009UB



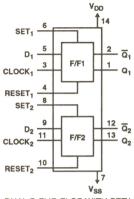
HEX BUFFER/CONVERTER, NON-INVERTING TYPE CD4010B



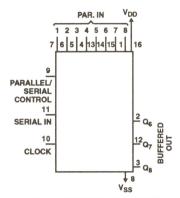
QUAD 2-INPUT NAND GATE CD4011B, CD4011UB



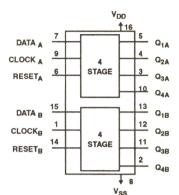
DUAL 4-INPUT NAND GATE CD4012B



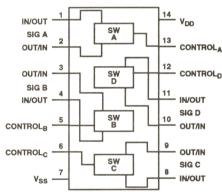
DUAL D FLIP-FLOP WITH SET/ RESET CAPABILITY CD4013B



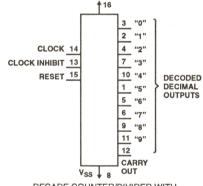
8-STAGE SYNCHRONOUS SHIFT REGISTER WITH PARALLEL OR SERIAL INPUT/SERIAL OUTPUT CD4014B



DUAL 4-STAGE STATIC SHIFT REGISTER WITH SERIAL INPUT/PARALLEL OUTPUT CD4015B

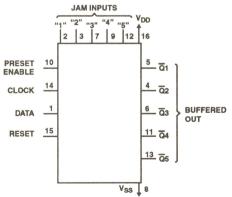


QUAD BILATERAL SWITCH CD4016B

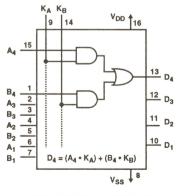


 V_{DD}

DECADE COUNTER/DIVIDER WITH 10 DECODED DECIMAL OUTPUTS CD4017B

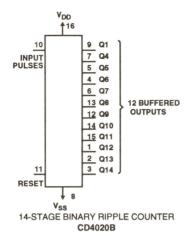


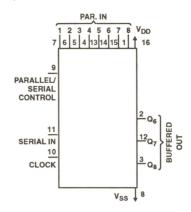
PRESETTABLE DIVIDE-BY-"N" COUNTER FIXED OR PROGRAMMABLE CD4018B



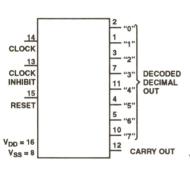
QUAD AND/OR SELECT GATE CD4019B

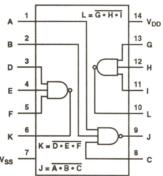
CD4000 CMOS Logic Functional Diagrams (Continued)

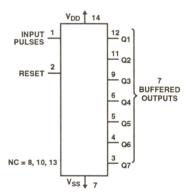




8-STAGE STATIC SHIFT REGISTER ASYNCHRONOUS PARALLEL
OR SYNCHRONOUS SERIAL INPUT/SERIAL OUTPUT
CD4021B

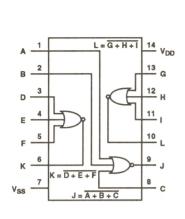


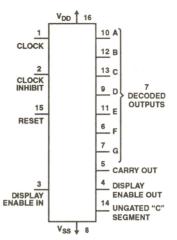


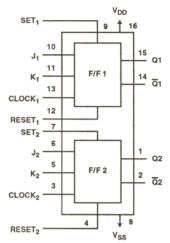


DIVIDE-BY-8 COUNTER/DIVIDER WITH 8 DECODED DECIMAL OUTPUTS CD4022B TRIPLE 3-INPUT NAND GATE CD4023B

7-STAGE RIPPLE-CARRY BINARY COUNTER/DIVIDER CD4024B



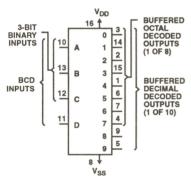




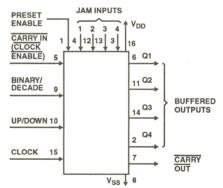
TRIPLE 3-INPUT NOR GATE CD4025B

DECADE COUNTER/DIVIDER WITH 7-SEGMENT DISPLAY OUTPUTS AND DISPLAY ENABLE CD4026B

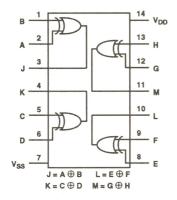
DUAL J-K MASTER-SLAVE FLIP-FLOP WITH SET-RESET CAPABILITY CD4027B



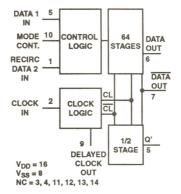
BCD-TO-DECIMAL DECODER CD4028B



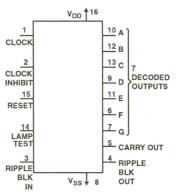
PRESETTABLE UP/DOWN COUNTER, BINARY OR BCD-DECADE CD4029B



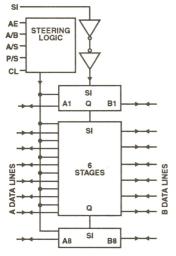
QUAD EXCLUSIVE-OR GATE CD4030B



64-STAGE STATIC SHIFT REGISTER CD4031B



DECADE COUNTER/DIVIDER WITH 7-SEGMENT DISPLAY OUTPUTS AND RIPPLE BLANKING CD4033B



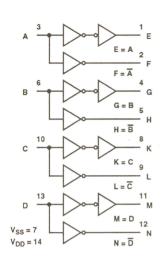
PARALLEL IN $\operatorname{SER} \left\{ \frac{\mathsf{J}}{\mathsf{K}} \right.$ CLK P/S T/C RESET 14 13 $V_{DD} = 16$ V_{SS} = 8 Q1/Q1 Q2/Q2 Q3/Q3 Q4/Q4 T/C OUT

V_{DD} 16 1 Q12 10 15 Q11 INPUT 14 Q10 PULSES 12 Q9 13 Q8 4 Q7 12-STAGE BUFFERED RIPPLE 2 Q6 **OUTPUTS** COUNTER 3 Q5 5 Q4 6 Q3 7 Q2 9 Q1 11 RESET V_{SS} ↓

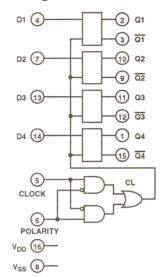
8-STAGE STATIC BIDIRECTIONAL PARALLEL/SERIAL INPUT/OUTPUT BUS SHIFT REGISTER WITH J-K SERIAL INPUTS REGISTER CD4034B

4-STAGE PARALLEL IN/PARALLEL OUT AND TRUE/COMPLEMENT OUTPUTS CD4035B

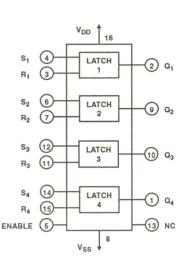
12-STAGE RIPPLE-CARRY BINARY COUNTER/DIVIDER CD4040B



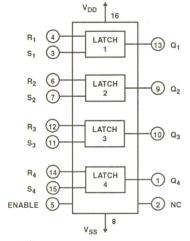




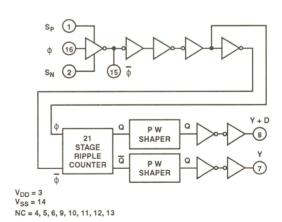
QUAD CLOCKED "D" LATCH CD4042B



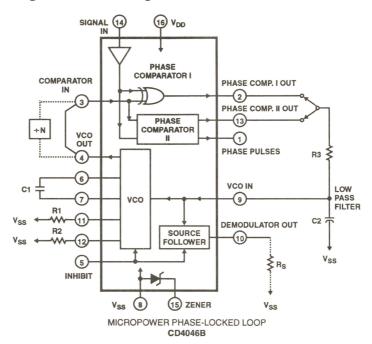
QUAD THREE-STATE NOR R/S LATCH CD4043B

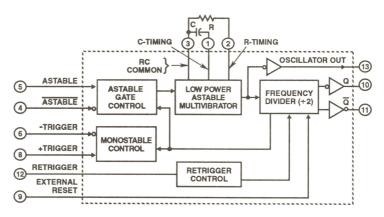


QUAD THREE-STATE NAND R/S LATCH CD4044B

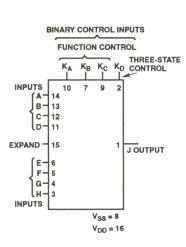


21-STAGE COUNTER CD4045B

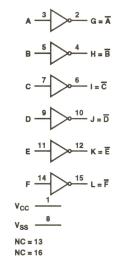




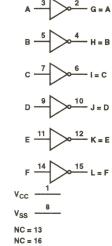
LOW-POWER MONOSTABLE/ASTABLE MULTIVIBRATOR CD4047B



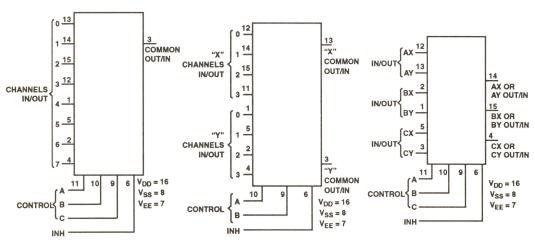
MULTI-FUNCTION EXPANDABLE 8-INPUT GATE CD4048B



HEX BUFFER/CONVERTER
INVERTING TYPE
CD4049UB

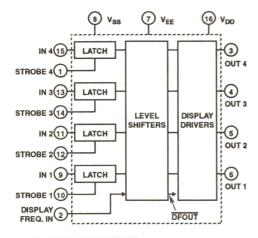


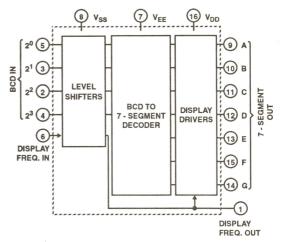
HEX BUFFER/CONVERTER NON-INVERTING TYPE CD4050B



SINGLE 8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER CD4051B DIFFERENTIAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER CD4052B TRIPLE 2-CHANNEL MULTIPLEXER/ DEMULTIPLEXER CD4053B

CD4000 CMOS Logic Functional Diagrams (Continued)

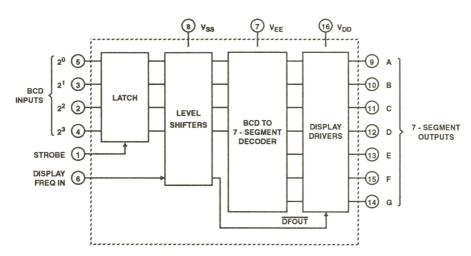




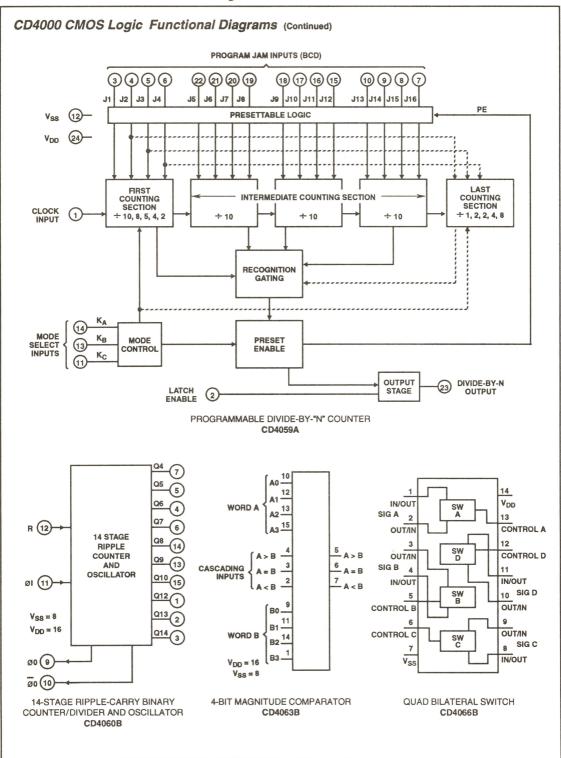
ALL INPUTS PROTECTED BY COS/MOS PROTECTION NETWORK

4-SEGMENT LIQUID CRYSTAL DISPLAY DRIVER CD4054B

BCD-TO-7-SEGMENT DECODER/DRIVER WITH
"DISPLAY-FREQUENCY" OUTPUT LIQUID-CRYSTAL
DISPLAY DRIVER
CD4055B

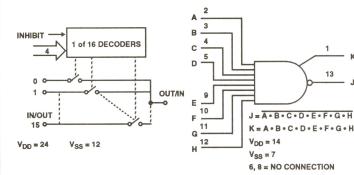


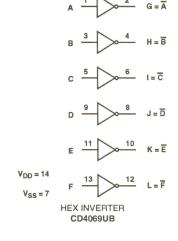
BCD-TO-7-SEGMENT DECODER/DRIVER WITH STROBED-LATCH FUNCTION LIQUID-CRYSTAL DISPLAY DRIVER CD4056B



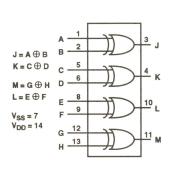
13

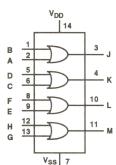
CD4000 CMOS Logic Functional Diagrams (Continued)





16-CHANNEL MULTIPLEXER/ DEMULTIPLEXER CD4067B



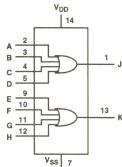


QUAD 2-INPUT OR GATE

CD4071B

8-INPUT NAND/AND GATE

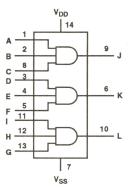
CD4068B



DUAL 4-INPUT OR GATE

CD4072B

QUAD EXECUTIVE-OR GATE CD4070B



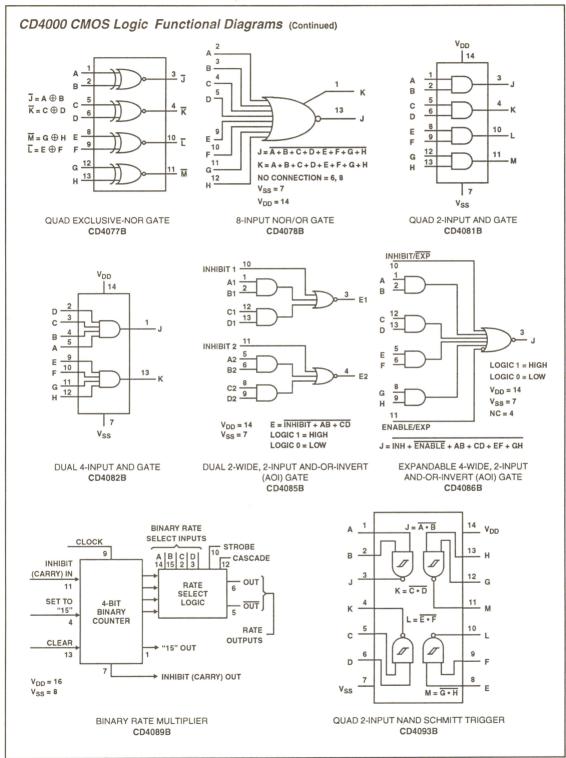
 V_{DD} 14 2 F 3 D 1 11 H 12 10 7 VSS

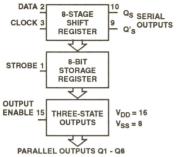
DATA INPUT OUTPUT DISABLE DISABLE G1 G2 CLOCK 10 2 | 7 D1 14 3 Q1 4 D-TYPE D2 13 FLIP/FLOP WITH D3 12 AND/OR 5 Q3 LOGIC D4 11 6 Q4 15 V_{SS} = 8 RESET V_{DD} = 16

TRIPLE 3-INPUT AND GATE CD4073B

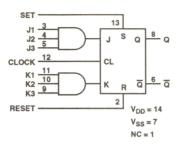
TRIPLE 3-INPUT OR GATE CD4075B

4-BIT D-TYPE REGISTER CD4076B

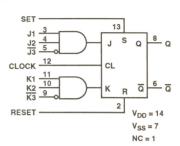




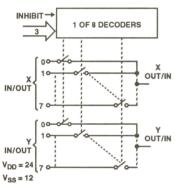
(TERMINALS 4, 5, 6, 7, 14, 13, 12, 11, RESPECTIVELY) 8-STAGE SHIFT-AND-STORE **BUS REGISTER** CD4094B



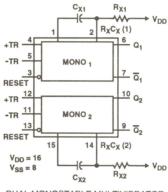
NON-INVERTING INPUTS CD4095B



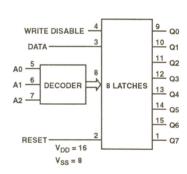
GATED J-K MASTER-SLAVE FLIP-FLOP, GATED J-K MASTER-SLAVE FLIP-FLOP, IN-VERTING AND NON-INVERTING INPUTS CD4096B



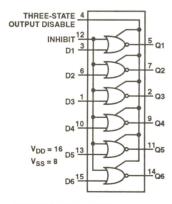
DIFFERENTIAL 8-CHANNEL MULTIPLEXER/DEMULTIPLEXER CD4097B



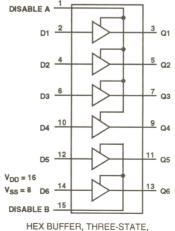
DUAL MONOSTABLE MULTIVIBRATOR CD4098B



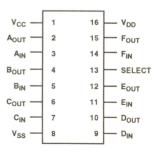
8-BIT ADDRESSABLE LATCH CD4099B



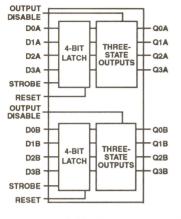
STROBED HEX INVERTER/BUFFER CD4502B



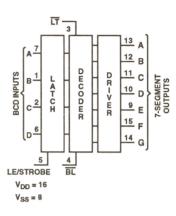
NON-INVERTING CD4503B



HEX VOLTAGE LEVEL SHIFTER CD4504B



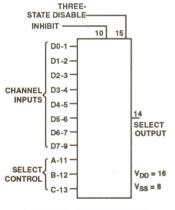
PRESET ENABLE 6 - Q1 11 Q2 12 P2 14 Q3 13 D2 3 2 Q4 P4 -15 CLOCK 10 UP/DOWN CARRY OUT CARRY IN 9 $V_{DD} = 16$ V_{SS} = 8 RESET



DUAL 4-BIT LATCH CD4508B

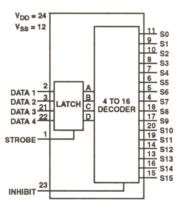
BCD PRESETTABLE UP/DOWN COUNTER CD4510B

BCD-TO-7-SEGMENT LATCH DECODER DRIVER CD4511B



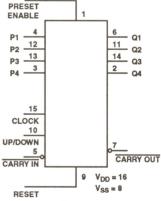
CD4512B



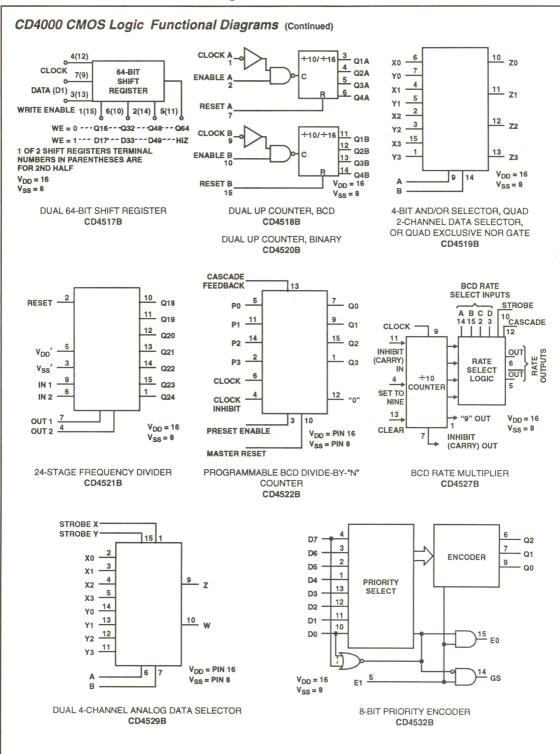


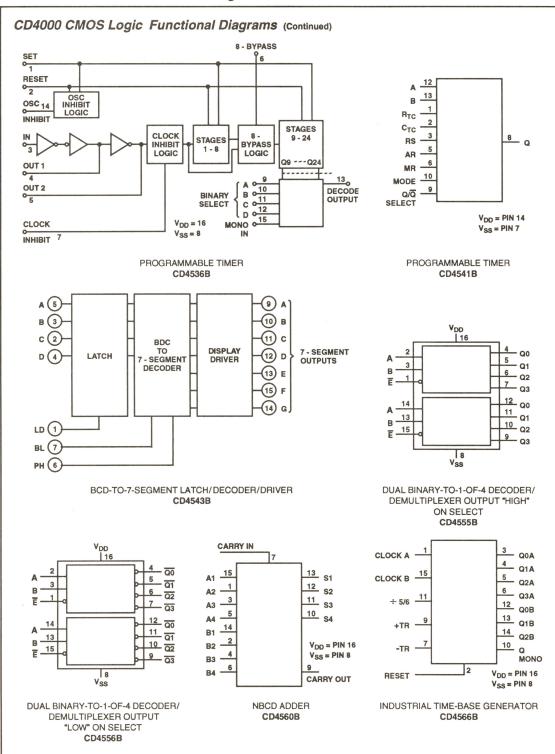
4-BIT LATCH/4-TO-16 LINE DECODER. **OUTPUT "HIGH" ON SELECT** CD4514B

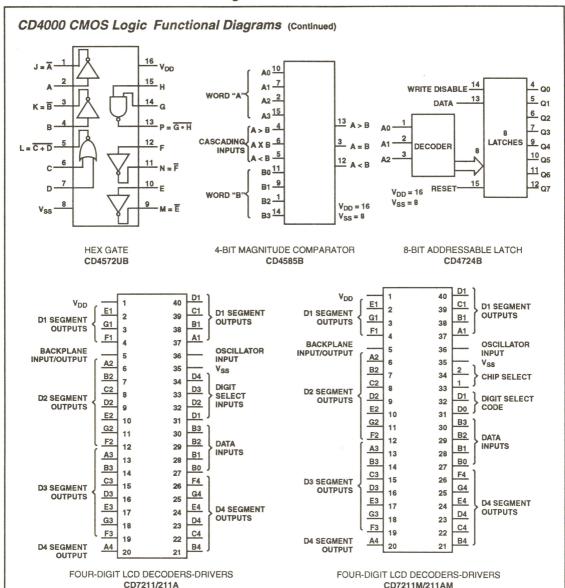




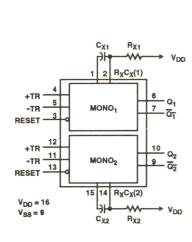
BINARY PRESETTABLE UP/DOWN COUNTER CD4516B

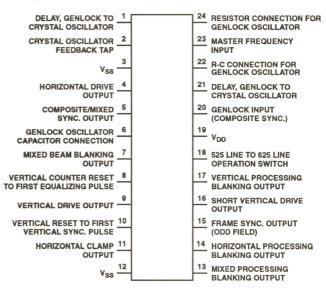






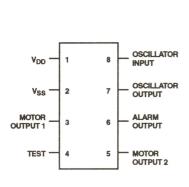
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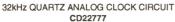


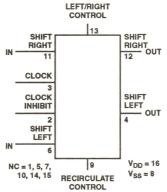


NOTE: PINS 3 AND 12 MUST BE TIED TOGETHER

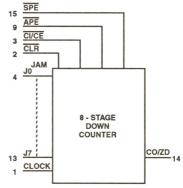
DUAL PRECISION MONOSTABLE MULTIVIBRATOR CD14538B LSI SYNC GENERATOR CD22402





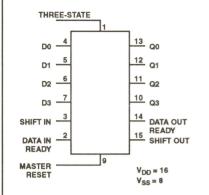


32-STAGE STATIC LEFT/RIGHT SHIFT REGISTER CD40100B

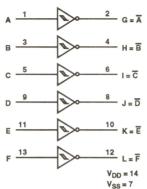


8-STAGE PRESETTABLE SYNCHRONOUS DOWN COUNTER, 2-DECADE BCD CD40102B

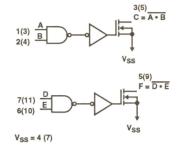
8-STAGE PRESETTABLE SYNCHRONOUS DOWN COUNTER, 8-BIT BINARY CD40103B



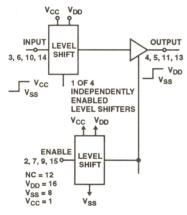
FIFO REGISTER 4-BITS WIDE BY 16-BITS LONG CD40105B



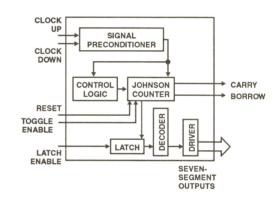
HEX SCHMITT TRIGGER CD40106B



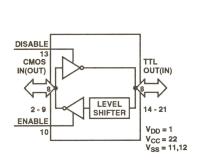
NOTE: Numbers in parentheses for CD40107BF, others for CD40107BE DUAL 2-INPUT NAND BUFFER/DRIVER CD40107B



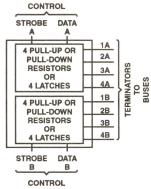
QUAD LOW-TO-HIGH VOLTAGE LEVEL SHIFTER CD40109B



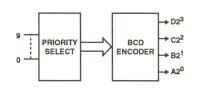
DECADE UP-DOWN COUNTER/DECODER/LATCH/DRIVER CD40110B



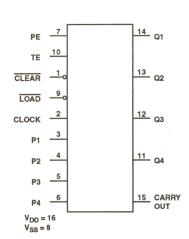
8-BIT UNIVERSAL BIDIRECTIONAL CMOS/TTL LEVEL CONVERTER CD40116



PROGRAMMABLE DUAL 4-BIT TERMINATOR CD40117B



10-LINE-TO-4-LINE BCD PRIORITY ENCODER CD40147B

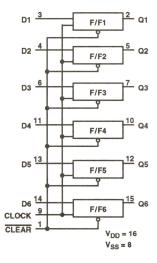


SYNCHRONOUS 4-BIT COUNTER, DECADE WITH ASYNCHRONOUS CLEAR CD40160B

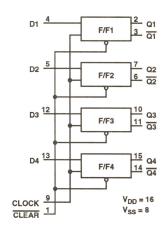


SYNCHRONOUS 4-BIT COUNTER, DECADE WITH SYNCHRONOUS CLEAR CD40162B

SYNCHRONOUS 4-BIT COUNTER, BINARY WITH SYNCHRONOUS CLEAR CD40163B



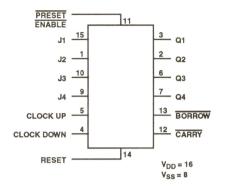
HEX D TYPE FLIP-FLOP CD40174B



QUAD D TYPE FLIP-FLOP CD40175B

Logic Selection Guide

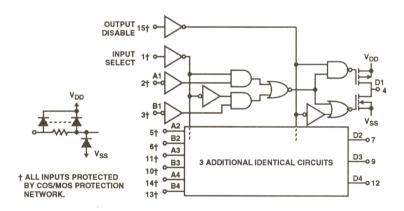
CD4000 CMOS Logic Functional Diagrams (Continued)



RESET 4 14 D1 Q1 5 13 D2 Q2 6 D3 12 SHIFT Q3 LEFT 7 IN SHIFT 2 RIGHT 9 MODE ∫ S₀ $V_{DD} = 16$ 10 SELECT V_{SS} = 8 CLOCK -

PRESETTABLE UP/DOWN CONVERTER (DUAL CLOCK WITH RESET), BCD CD40192B

PRESETTABLE UP/DOWN CONVERTER (DUAL CLOCK WITH RESET), BINARY CD40193B 4-BIT UNIVERSAL BIDIRECTIONAL SHIFT REGISTER
WITH ASYNCHRONOUS MASTER RESET
CD40194B



QUAD 2-LINE-TO-1-LINE DATA SELECTOR/MULTIPLEXER CD40257B

CMOS LOGIC ICS

PRODUCT SELECTION GUIDE

HIGH SPEED CMOS LOGIC - HC/HCT SERIES

	PAGE
TECHNICAL OVERVIEW	2-3
Description	2-3
Features	2-3
IC Structure.	2-4
Input Characteristics.	2-5
Latch-Up	2-8
Output Characteristics	2-9
Dynamic Characteristics	2-13
Power Consumption	2-15
Power-Supply Considerations	2-17
Interfacing	2-18
Bus Systems.	2-20
Standardized Capacitance Power Dissipation (C _{PD}) Test Procedure	2-21
FAMILY RATINGS AND SPECIFICATIONS‡	2-28
Switching Waveforms for CD54/74HC and CD54/74HCU Integrated Circuits	2-30
Switching Waveforms for CD54/74HC and CD54/74HCT Integrated Circuits	2-31
OPERATING AND HANDLING CONSIDERATIONS	2-32
ENHANCED PRODUCT	2-32

For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX. See Section 8, "How to use AnswerFAX", in this selection guide.

Description

The Harris HC/HCT series of high speed CMOS integrated circuits (QMOS) includes a functionally complete set of LSTTL equivalent types and selected equivalent CMOS CD4000 series types. The CD4000 series types selected are unique to the CMOS process. These types are readily produced by the highly versatile CMOS technology, but cannot be implemented by the more restrictive bipolar technology. Each CMOS circuit function is offered in two basic logic series, as follows:

CD54/74HCTXXXX-Series Types. These feature LSTTL input voltage level compatibility and provide high speed CMOS direct drop-in replacements of LSTTL devices.

CD54/74HCXXXX-Series Types. These feature CMOS input voltage level compatibility and are intended for use in new second generation all CMOS systems.

In addition, Harris offers a third category, CD54/74HCUXX, which includes unbuffered types intended for linear or high speed oscillator applications.

The HC/HCT family consists of a comprehensive set of buffers, transceivers, and registers that are popular in computer systems. A wide variety of popular logic, MUXs, encoders/decoders, counters, arithmetic units, mulitvibrators, display drivers, and phase-lock loops complete the family.

Shown below is a breakdown of the HC/HCT family by logic function:

THE HC/HCT FAMILY

Device Function

- · Inverters/Buffers/Bus Drivers
- Flip-Flops/Latches
- Bus Transceivers
- Registers
- Counters
- · Decoders/Encoders
- · Multiplexers (Analog and Digital)
- Multivibrators
- · Schmitt Triggers
- · Phase-Lock Loops
- Bilateral Switches
- · Arithmetic Circuits
- Gates

NOTE: Each function is available in both an HCT and HC version.

Features

- Functionally and Pin Compatible with Industry 54 and 74 LSTTL-Series and CD4000B-Series Types
- · CMOS Outputs for Maximum Noise Margins
- Fanout (Over Temperature): Standard Outputs - 10 LSTTL Loads Bus-Driver Outputs - 15 LSTTL Loads

- Wide Operating Temperature Ranges
 CD74HC/HCT/HCU......55°C to +125°C
 CD54HC/HCT/HCU.....55°C to +125°C
- · Balanced Propagation and Transition Times
- · Significant Power Reduction Compared to LSTTL Logic

Series Features

CD54HCXXXX and CD74HCXXXX Series

- · 2V to 6V Operation
- High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% at V_{CC} = 5V CD54HCTXXXX and CD74HCTXXXX Series
- · 4.5V to 5.5V Operation
- Direct LSTTL Input Logic Compatibility: V_{IL} 0.8V(Max), V_{IH} = 2.0V (Min)
- CMOS Input Compatibility: I_{IL}, I_{IH} ≤1μA at V_{OL}, V_{OH}

Quantitative Comparison of HC/HCT and LSTTL Logic Types

Harris HC and HCT logic types have many outstanding advantages when compared with the conventional high current LSTTL logic types which these types can replace in existing and new equipment designs that require devices operating at frequencies in the 20MHz to 30MHz range. Table 1 compares significant operating characteristics of the HC/HCT vs LSTTL logic families.

TABLE 1. QUANTITATIVE COMPARISON OF HC/HCT AND LSTTL LOGIC TYPES

74 SERIES HC/HCT		74 SERIES LSTTL				
0.02	5mW	5.5	mW			
0.05	SmW	101	nW			
0.4	mW	951	nW			
0.1	mW	601	nW			
OPERATING POWER						
FREQUENCY			JENCY			
1MHz	10MHz	0.1 to 1MHz	10MHz			
2mW	20mW	5.5mW	20mW			
1.5mW	15mW	10mW	15mW			
2.4mW 24mW		95mW	120mW			
2.5mW	25mW	60mW	90mW			
	0.02 0.08 0.4 0.1 REQUENC 1MHz 2mW 1.5mW	0.025mW 0.05mW 0.4mW 0.1mW REQUENCY 1MHz 10MHz 2mW 20mW 1.5mW 15mW 2.4mW 24mW	0.025mW 5.5i 0.05mW 10i 0.4mW 95i 0.1mW 60i 0.1mW 10mHz 10mHz 10mHz 1.5mW 1.5mW			

(HC) 2V to 6V (HCT) 4.5V to 5.5V

4.75V to 5.25V

TABLE 1. QUANTITATIVE COMPARISON OF HC/HCT AND LSTTL LOGIC TYPES (Continued)

PARAM	ETERS	74 SERIES HC/HCT	74 SERIES LSTTL
OPERATING	TEMPERAT	URE RANGE	
		-40°C to +85°C	0°C to +70°C
NOISE MARG	OINLAT EV	_	
LS to LS	(Hi/Low)		0.7V/0.4V
	(FILLOW)	1 41//1 41/	0.7 7/0.47
HC to HC	-	1.4V/1.4V	-
HCT to HCT		2.9V/0.7V	-
INPUT SWITE	CHING VOLI	AGE VARIATION WI	
was Madimus areawan Manaksumia kinga		V _S ± 60mV	V _S ± 200mV
OUTPUT DR	IVE CURREN	NT	
Source Curre V _{OH} = 2.4V	nt at	-8mA	-400μA
Sink Current	Std. Logic (V _{OL})	4mA (0.33V)	4mA (0.4V)
	BUS Logic (V _{OL})	6mA (0.33V)	12mA (0.4V)
	$V_{OL} = 0.5V$	12mA	24mA
TYPICAL OU	TPUT TRAN	SITION TIME (Note	1)
t _{TLH}		6ns	15ns
t _{THL}		6ns	6ns
TYPICAL GA	TE PROPAG	ATION DELAY (Not	e 1)
t _{PHL} /t _{PLH} V _{CC} = 5V,C _L	= 15pF	8ns/8ns	8ns/11ns
TYPICAL FF	PROPAGAT	ION DELAY	
t _{PHL} V _{CC} = 5V,C _L	= 15pF	14ns	22ns
t _{PLH} V _{CC} = 5V,C _L		14ns	15ns
TYPICAL CL	OCK RATE C	F AN FF	
		50MHz	33MHz
INPUT CURF	RENT	L	
I _{IL}		-1μΑ	-0.4mA to -0.8mA
I _{IH}		1µА	40µА
	TE OUTPUT	LEAKAGE CURREN	
		±5μA	±20μΑ
RELIABILITY		pa 1	
%/1000 hours		0.0019	0.008
Confidence		Harris Report	RADC Report

NOTE:

1. Loading coefficient = 0.055ns/pF (both HC/HCT and LSTTL).

IC Structure

The high speeds and low quiescent power dissipation that characterize the Harris HC/HCT family are made possible by utilizing a 3μ , self-aligned silicon gate CMOS process. The 3μ process minimizes the internal parasitic capacitances of the circuit, which results in increased switching speed.

The polysilicon gates of the transistors are deposited over a thin gate oxide before the source and drain diffusions are defined. Ion implantation is then used to form the source and drain areas, with the polysilicon gates acting as a mask for the implantation. The source and drain are automatically aligned to the gate, hence the expression "self-aligned-gate" process. In this manner, gate-to-source and gate-to-drain capacitances are minimized. Junction capacitances, which are proportional to the junction area, are also reduced because of the shallower diffusions. Figure 1 shows the parasitic capacitances in a CMOS inverter.

In contrast, the source and drain areas in a metal-gate CMOS process are formed before the gate is deposited.

Moreover, the metal gate must overlap the source and drain to allow for alignment tolerances. These conditions result in higher overlap capacitances than those present in QMOS devices. The metal-gate process also employs deeper diffusions than those in the QMOS process and, consequently, has larger junction capacitances.

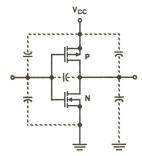


FIGURE 1. PARASITIC CAPACITANCES IN A CMOS INVERTER

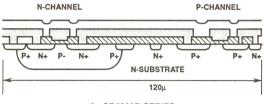
The QMOS structure features a 3μ gate length; the CD4000 series structure has a gate length of $7\mu.$ The equation for the drain current of a MOSFET is:

$$I_{DS} = K' \frac{\text{width}}{\text{length}} [(Gate Voltage) - (Threshold Voltage)]^2$$

where K ' is the "beta" of the MOSFET. Therefore, a shorter gate length results in higher drive capability, which in turn increases the speed at which a transistor can charge or discharge capacitance.

The polysilicon in a silicon-gate process is also an interconnect layer, thus, there are three levels of interconnect (diffusion, polysilicon, and metal) instead of the two layers (diffusion and metal) present in a metal gate process. This

situation aids in making a more compact die. Figure 2 compares the cross sections of the 7μ metal-gate CMOS structure and the 3μ QMOS structure.



A. CD4000B SERIES

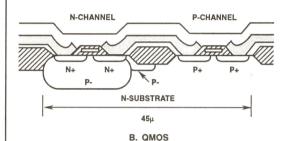


FIGURE 2. CROSS-SECTIONAL VIEW OF:

- (A.) 7μ CD4000B SERIES STRUCTURE
- (B.) 3µ QMOS STRUCTURE

Input Characteristics

The inputs of QMOS devices are voltage level sensitive, and do not require current, except for input leakage. The definitive switching characteristics for the HC and HCT versions are illustrated in Figure 3 and Figure 4, respectively.

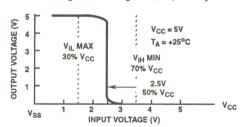


FIGURE 3. TYPICAL SWITCHING CHARACTERISTICS OF HARRIS HC SERIES TYPES

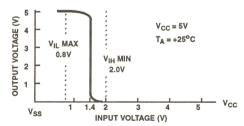


FIGURE 4. TYPICAL SWITCHING CHARACTERISTICS OF HARRIS HCT SERIES TYPES

System designers require the actual Min/Max range of expected input switching voltage over the temperature range of -55°C to +125°C. This vital information is contained in the curves of Figure 5 and Figure 6 for the HC and HCT families, respectively.

The unbuffered HCU04 hex inverter has one stage of active inverting logic from input to output and, therefore, is a special case for input switching voltage as shown in Figure 7.

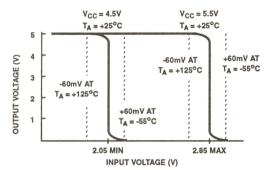


FIGURE 5. ACTUAL MIN/MAX SWITCHING CHARACTERISTICS
OF HARRIS HC SERIES TYPES

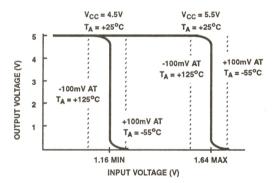


FIGURE 6. ACTUAL MIN/MAX SWITCHING CHARACTERISTICS
OF HARRIS HCT SERIES TYPES

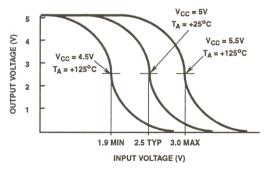


FIGURE 7. ACTUAL MIN/MAX AND TYPICAL SWITCHING
CHARACTERISTICS OF THE HCU04 UNBUFFERED
HEX INVERTER

Noise Immunity and Noise Margin

Table 2A shows the HC, HCT, and HCU input noise immunity and noise margin for use in those applications where like members of the HC, HCT, and HCU families interface with each other at a nominal supply voltage of 5V. Output voltages are also shown.

TABLE 2A. NOISE IMMUNITY AND NOISE MARGIN ($V_{CC} = 5V$)

	нс	нст	HCU
V _{IL} Max	1.5V	0.8V	1V
V _{IH} Min	3.5V	2V	4V
V _{OL} Max	0.1V	0.1V	0.5V
V _{OH} Min	4.9V	4.9V	4.5V
Noise Margin Low (V _{NML})	1.4V	0.7V	0.5V
Noise Margin High (V _{NMH})	1.4V	2.9V	0.5V

Table 2B shows noise immunity and noise margin voltages for standard HCT devices interfacing with LSTTL logic types with a fully loaded HCT or LSTTL output at $\rm V_{CC}=4.5V$, and a temperature range of 0°C to +70°C. This limited LSTTL temperature range is the only convenient temperature range when using LSTTL characteristics.

Whenever the HCT output drives either an LS or HCT input, there is an improvement in noise margin over the LSTTL family driving itself or driving HCT. This improvement is especially true for noise margin high where the superior output sourcing current of the rail-to-rail QMOS output swing is far superior to the limited totem-pole pull-up output voltage of LSTTL.

TABLE 2B. NOISE IMMUNITY AND NOISE MARGIN FOR HCT AND LS DEVICE INTERFACING

	нст	LSTTL	HCT→LS	LS→HCT	LS→LS	нст⊸нст
V _{IL} Max	0.8V	0.8V	-	-	-	-
V _{IH} Min	2V	2V	-	-	-	-
V _{OL} Max	0.33V	0.4V	-	-	-	-
V _{OH} Min	4.4V	2.7V	-	-	-	-
V _{NML}	-	-	0.47V	0.4V	0.4V	0.7V
V _{NMH}	-	-	2.4V	0.7V	0.7V	2.4V

Input Current

Figure 8 is a plot of typical HC/HCT device input current vs. temperature for a $V_{\rm CC}$ of 6V. This actual performance of under 1.5nA over the temperature range of -55°C to +125°C contrasts with maximum family and JEDEC standard input leakage current limit of 100nA for T = -55°C to +25°C, and a limit of 1µA at $T_{\rm A}$ = +85°C and +125°C. The reason for this difference in performance vs ratings is high speed testing limitations associated with test system resolution and the measurement of settling time. A secondary reason is that the limits are end-of-life, thus allowing some leakage current shift due to minor externally introduced foreign material or moisture.

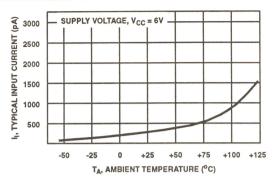


FIGURE 8. TYPICAL HC/HCT INPUT CURRENT vs TEMPERATURE Input Termination

The very low HC/HCT input current and hence, high input resistance is primarily due to low-level leakage currents of the input ESD protection diodes shown in Figure 9. This excellent input buffering characteristic of CMOS logic ICs is fundamental to the wide range of very low power applications from pure logic to wide range RC oscillators, high Q crystal oscillators, etc. However, in no situation should this high input resistance be left floating or unterminated. Inputs may be tied directly to V_{CC} or GND via resistors of up to $1\text{M}\Omega$; the upper limit is only related to AC noise immunity, i.e., pick up.

Comparing HC/HCT unused input terminations to LSTTL logic, puts the flexibility of QMOS into a very positive light. It is a stated LSTTL design rule that unused inputs be terminated to V_{CC} via a 1.2k Ω resistor and not tied directly to GND or V_{CC} nor left floating.

One additional note on HC/HCT input terminations. There are several bidirectional (transceiver) logic types in the QMOS family with common I/O pins. These I/O pins do not have the input poly resistor (R) of Figure 9. Hence, these pins cannot be terminated directly to $V_{\rm CC}$ or GND. A terminating resistor to $V_{\rm CC}$ or GND of $10 k\Omega$ is recommended.

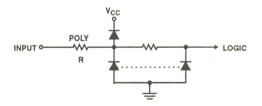


FIGURE 9. RESISTOR DIODE PROTECTION NETWORK USED ON INPUTS OF HC/HCT DEVICES TO PROTECT DEVICE GATE OXIDE FROM ELECTROSTATIC DISCHARGE DAMAGE (ESD)

Input/Output ESD Protection

HC/HCT device inputs have a resistor-diode protection network, shown in Figure 9, that protects the gate oxide from electrostatic discharge (ESD) damage. The network provides protection to levels typically greater than 2kV in all modes pertaining to the input, as shown in Figure 10. The

2kV figure was arrived at by testing devices in the ESD test circuit shown in Figure 11 while conforming to the MIL-I-38535 requirements.

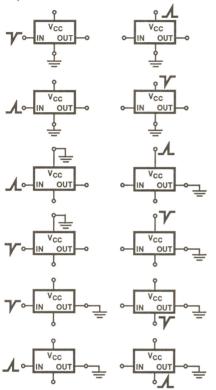


FIGURE 10. HC/HCT ESD TEST MODES

The recommended handling practices for QMOS devices are similar to those described in Application Note AN6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits". See Section 8, "How to Use AnswerFAX", of this selection guide.

C_H = HUMAN BODY CAPACITANCE TO GROUND R_S = BODY SOURCE RESISTANCE

FIGURE 11. TEST CIRCUIT USED TO MEASURE ELECTRO-STATIC DISCHARGE (ESD) IN HC/HCT CIRCUITS. THE RISE TIME AT THE OUTPUT TERMINAL SHOULD BE 13ns ± 2ns

Input Interaction

Another effect of the input-protection network is the imposition of a parasitic transistor between adjacent input pins. Figure 12 shows this transistor.

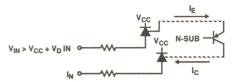
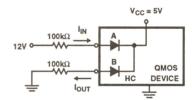


FIGURE 12. PARASITIC TRANSISTOR CAUSED BY INPUT-PROTECTION NETWORK

This parasitic transistor may cause undesirable interaction between adjacent inputs if the input level is greater than $V_{CC}+V_{DIODE}.$ QMOS devices minimize the alpha (\approx = I_E/I_C) to less than 0.05. This feature of QMOS inputs permits proper logic operation in the presence of transients and also allows high to low voltage translation via series input resistors. The typical value of \approx for QMOS ICs is 0.001. Figure 13 illustrates how control of \approx in QMOS devices provides for safe conversion of 12V control logic levels to 5V HC system logic simply by insertion of a 100k Ω resistor in each input. The only disadvantage is that logic signals are delayed by 1 μ s to 2 μ s and therefore, this scheme works well only with rather slow 12V control logic as for example, in automotive applications. When the input diodes are used as clamps for logic level translation, the input current should be kept to 2mA or less.



$$I_{I} = \frac{6.3V}{100 k\Omega} = 63 \mu A$$
 $I_{O} = \infty I_{I} = 0.05 \times 63 \mu A = 3.15 \mu A$
 $V_{IL(B)} = 3.15 \mu A \times 100 k\Omega = 0.315 V$
 $V_{IL}MAX(SPEC) = 1.5 V$

NOISE MARGIN = 1.5V - 0.315V = 1.2V APPROX

FIGURE 13. 12V TO 5V LOGIC LEVEL CONVERSION AT HC IN-PUTS USING $100 \mathrm{K}\Omega$ SERIES RESISTORS

Input-Voltage Considerations and Maximum Forward-Diode Input Current Limits

As a general rule, CMOS logic devices employing input clamp diodes (Figure 9) to minimize ESD effects should be operated between the power supply rails. If the input series polysilicon resistor shown in Figure 9 is not considered, then the rule is: $-0.5V \le V_{\text{IN}} \le (V_{\text{CC}} + 0.5V)$.

This rule is the industry standard (JEDEC Std. No. 7) and is intended to keep users from damaging devices because the devices of some HC/HCT device manufacturers do not have the built-in input series polysilicon resistor. Harris HC/HCT data sheets continue to show the conservative rating established by JEDEC. However, Harris HC/HCT device inputs are capable of meeting the following rating:

$$-1.5V \le V_{IN} \le V_{CC} + 1.5V.$$

Furthermore, Harris devices, except for special cases such as transceivers and analog switches or multiplexer signal inputs, can reliably operate with the ±1.5V rule without logic errors. Beyond ±1.5V, maximum forward current poses a second limitation with respect to the V_{CC} and GND rail. This QMOS and JEDEC rating is ±20mA of transient current maximum forced into inputs or outputs.

Latch-Up

Definition

Latch-up within CMOS IC structures may be initiated or triggered by voltage overshoot or undershoot at inputs, outputs, or supply terminals. A high transient voltage or current at any one or combination of these terminals may initiate turn-on of an SCR-type 4-layer diode parasitic bipolar device, as shown in the simplified diagram of Figure 14. This parasitic structure, when triggered on, keeps the supply voltage below the V_{CC} voltage and thus permits a high supply current of several hundred mA to flow (see Figure 14). The resistor values of r_C, r_{BB}⁻¹, r_{BB}⁻² are dependent on circuit layout geometry and p+ and n+ doping levels.

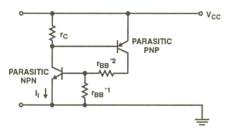


FIGURE 14. SIMPLIFIED DIAGRAM OF CMOS 4-LAYER DIODE STRUCTURE

The lower the value of these resistors, the less voltage drop that will occur. A much higher trigger current, therefore, will be required to induce turn on of the SCR structure shown in Figure 14.

Also important are established layout rules and process parameters that minimize the current gain (Beta) of the parasitic NPN and PNP transistors shown in Figure 14.

Latch-Up Capability

The trigger current that could potentially trigger latch-up of QMOS ICs is typically ± 80 mA at any input or output terminal. Measurements are made at all terminals (see next section for preferred measurement technique), so that these terminals have a minimum acceptable latch current of ± 40 mA. The absolute maximum rating in the QMOS data sheet and

in the industry JEDEC Standard No. 7 is ± 20 mA. The possibility for transient currents in applications are more likely to appear at input terminals where interfaces could cause voltage transients. The voltage required to induce the ± 40 mA measured capability and the ± 80 mA typical capability of QMOS ICs as illustrated in Figure 15, is established by the QMOS built-in 120Ω minimum current-limiting polysilicon resistor at logic inputs.

Equations:

$$V_T = I_T R + V_D + V_{CC}$$
 $R = 120\Omega$
 $-V_T = -I_T R - V_D$ $V_{CC} = 4.5V$

Values:

$$V_T = 40 \text{mA} \times 0.12 \text{K}\Omega + 0.7 \text{V} + 4.5 \text{V} = 10 \text{V} \text{ Min}$$
 $V_T = 80 \text{mA} \times 0.12 \text{K}\Omega + 0.7 \text{V} + 4.5 \text{V} = 14.8 \text{V} \text{ Typ}$
 $-V_T = -40 \text{mA} \times 0.12 \text{K}\Omega - 0.7 \text{V} = -5.2 \text{V} \text{ Min}$
 $-V_T = -80 \text{mA} \times 0.12 \text{K}\Omega - 0.7 \text{V} = -10.3 \text{V} \text{ Typ}$

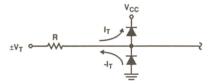


FIGURE 15. INPUT LATCH TRANSIENT VOLTAGE
DETERMINATION

As developed in Figure 15, the minimum and typical $\pm V_T$ transient input voltages required to induce either ±40mA or ±80mA are relatively large, and far greater than the transients induced in 5V systems where 2V or 3V of ringing transients can be induced via wiring inductance effects. This ±40mA QMOS capability is truly a "latch-up free" condition for operation in a 2V to 6V system. If transients are induced in a particular application beyond +10V/-5.2V, then the use of external series-limiting resistors are advised to keep transient currents below ±40mA. Another consideration is unused inputs. If unused QMOS inputs are tied to a V_{CC} of +5.5V and the V_{CC} of the QMOS IC is temporarily grounded, for example, in a 2-power supply system, or when PC cards are replaced with power on, no possibility of latch-up will exist because the input current will be limited to ±40mA via the built-in 120Ω polysilicon series resistor.

Measuring Latch-Up Sensitivity

The test methods that follow can damage devices if the following precautions are not strictly observed.

- · Apply currents for 1ms Min to 5s Max.
- · Limit power supply currents to 200mA.
- Allow a cool-down period between successive tests to be equal to or greater than the time that is required to apply trigger current.
- These tests may be safely adapted to bench-testing with meters or use of a curve tracer.

1. Static Input or Output Triggering for Latch-up

V_{CC} Supply to 200mA

For input triggering, connect other inputs to V_{CC} or GND All valid logic conditions are subject to test.

For Output Triggering (Figure 16C and Figure 16D)

- · -IO Active Outputs Must Be Set Low
- +IO Active Outputs Must Be Set High
- Three-State Outputs Also Set Output To High Impedance State

Apply trigger current first (Figure 17)

- Apply ±I₁ or ±I_O (Figure 16)
- Raise V_{CC} to ±V_{CC} Max
- · After the Trigger Duration, Reduce Trigger Current to Zero
- If I_{CC} is Less than Its Quiescent Value, the Device is not Latched.

If the quiescent value of $I_{\rm CC}$ is out of specification, the input and output structure should be electrically checked to determine if the I/O circuitry is damaged and latch-up did not occur. Further device analysis may be required to verify if latch-up did indeed occur.

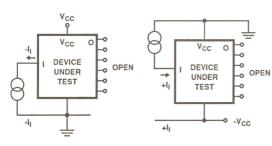


FIGURE 16A.

FIGURE 16B.

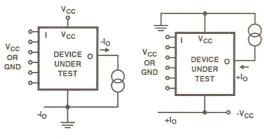


FIGURE 16C.

FIGURE 16D.

FIGURE 16. TEST SET-UP FOR POSITIVE AND NEGATIVE TRIGGER CURRENT

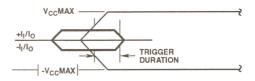


FIGURE 17. LATCH TEST WAVEFORMS

V_{CC} Triggered Latch-Up Test by Over-Voltage on V_{CC} (Figure 18)

Latch-up can occur if the voltage of the power supply is raised above the absolute maximum supply voltage rating.

Apply a V_{CC} over-voltage of 2X V_{CC} Max referenced to GND using a 100mA limited supply.

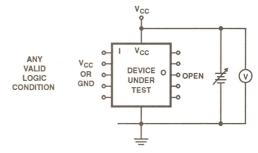
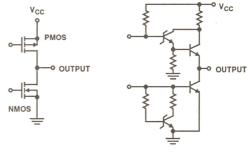


FIGURE 18. TEST SET-UP FOR V_{CC} OVER-VOLTAGE LATCH

Measure the V_{CC} voltage. If it is less than V_{CC} Max, the part has latched.

Output Characteristics

QMOS outputs make use of a complementary symmetry transistor configuration, which is different from the LSTTL totem-pole output; both outputs are shown in Figure 19. QMOS outputs meet the voltage level requirements necessary to interface to QMOS inputs, and the drive and current requirements needed to interface to bipolar inputs; i.e., TTL, LS, ALS, AS, FAST, etc.



A. CMOS OUITPUT

B. LSTTL OUTPUT

FIGURE 19. COMPARISON OF HC/HCT (A.) AND LSTTL (B.)

The outputs of the QMOS devices are classified into two categories: standard and bus drive. The two outputs differ in the output transistor widths needed to meet JEDEC standard drive and current requirements. Both standard outputs and bus drive outputs may be active (two-state) or three-state with a high-impedance mode added and where both the PMOS and NMOS transistors are off. Another type of QMOS output is the open-drain output of the HC/HCT 03 Quad NAND gate shown in Figure 20. This output has no intrinsic or added diode connected to V_{CC} at the output. The output of this device may be connected to an external load terminated at up to 10V. Thus, outputs can be pulled up above a nominal 5V supply for up-level voltage conversion.

The HC/HCT03 is the only QMOS gate type whose outputs can be used for a "wired OR" arrangement.

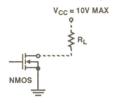


FIGURE 20. HC/HCT 03 OUTPUT CIRCUIT

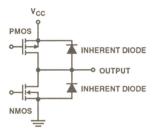


FIGURE 21. INHERENT DIODES PROTECTING HC/HCT OUTPUTS

Output Protection

The outputs in a QMOS device are protected from ESD damage by diodes. Figure 21 shows these diodes. These intrinsic diodes are effective because of the large geometries (widths) of the output transistors. These diodes are the drain to n-substrate junction of the p device and the drain to p-well junction of the n device. This network provides protection to voltage levels typically greater than 3kV in all ESD discharge modes pertaining to the output (see Figure 10).

Output Currents

QMOS outputs are specified for both CMOS and LSTTL loads. CMOS inputs are voltage sensitive and the only current is leakage current. The output voltage test for CMOS interfacing is specified for I_{O} at $\pm 20 \mu A$ (20 CMOS loads). The outputs are also specified at I_{O} = 4mA (10 LSTTL loads) and 6mA (15 LSTTL loads) for standard and bus-drive outputs, respectively. The corresponding V_{OL} Max and V_{OH} Min for the outputs, are illustrated in Table 3.

The maximum current per output pin I_O is ± 25 mA and ± 35 mA for standard and bus-drive outputs, respectively. This maximum current rating is specified when the outputs are in their active regions: -0.5V < V_O < V_{CC} + 0.5V. The maximum current rating per power pin, V_{CC} or ground, is 50mA and 70mA, respectively, for standard or bus-drive outputs.

When the output voltage exceeds V_{CC} or is below ground by greater than 500mV, the output protection diodes turn on and conduct current. The maximum diode transient current, I_{OK} , should not exceed ± 40 mA to avoid latch-up as described earlier.

TABLE 3. OUTPUT DRIVE SPECIFICATIONS

		TEST CONDITIONS/LIMITS (V _{CC} 4.5V)					
PARAMETER	SYMBOL	l _o	+25°C	-40°C to +85°C	-55°C to +125°C	UNIT	
High-Level Output	V _{OH} Min	-20μΑ	4.4	4.4	4.4	٧	
Voltage		-4mA	3.98	3.84	3.7	٧	
		-6mA (Bus)	3.98	3.84	3.7	٧	
Low-Level	V _{OL} Max	20μΑ	0.1	0.1	0.1	٧	
Output Voltage		4mA	0.26	0.33	0.4	V	
		6mA (Bus)	0.26	0.33	0.4	٧	

Output-Current and Interfacing Capability

A comparison of the output drive capabilities for QMOS with those of LSTTL is as follows:

LSTTL capability is usually expressed in unit loads (ULs) where the load is specified to be an input of the same family. This specification assures that the worst case low and high input thresholds will be met and the existing margins of noise immunity preserved.

QMOS capability is expressed as source/sink current at a specified output voltage. Since QMOS requires virtually no input current, the unit load concept does not apply.

With a specified output drive of 0.4mA at 0.4V, the QMOS to QMOS interface capability exceeds 1000ULs, and with a 20 μ A/0.1V specification, the QMOS capability is 20ULs. Each standard QMOS output has a drive capability of ten LSTTL loads and maintains a V_{OL} of 0.4V over the full temperature range. Bus driver outputs can drive 15 LSTTL loads under the same conditions.

TABLE 4. COMPARISON OF OUTPUT DRIVE CAPABILITIES

LS DEVICE	OUTPUT DRIVE	HC/HCT EQUIVALENT	OUTPUT TYPE	ОИТРИТ	DRIVE
74LS00	4mA 10UL	74HC00	Standard	4mA	10UL
74LS138	4mA 10UL	74HC138	Standard	4mA	10UL
74LS245	12mA 30UL	74HC245	Bus	6mA	15UL
74LS374	12mA 30UL	74HC374	Bus	6mA	15UL

The output drive capabilities of QMOS expressed in LSTTL unit loads are shown in Table 4.

Output Curves

Output current derating versus temperature is shown in Figure 22 and is valid for all types of output. Output source and sink drives at $V_{\rm CC}=2V$, 4.5V, and 6V are given in Figure 23 to Figure 26 which show output currents versus output voltages. These curves indicate the typical output current at +25°C and minimum output currents that can be expected at +25°C, +85°C, and +125°C, and can also serve as a design aid in interface applications and for calculating transmission line effects on charging highly capacitive loads.

Note to Figure 22 to Figure 25: The expected minimum curves are included as an aid to equipment designers, and are tested only at the points indicated on device data sheets.

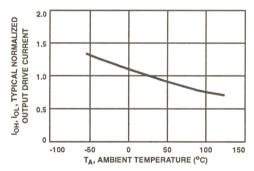
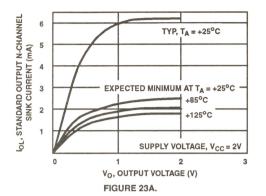


FIGURE 22. OUTPUT CURRENT DERATING VS AMBIENT TEMPERATURE



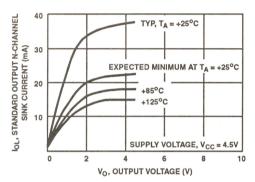


FIGURE 23B.

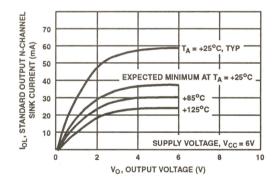
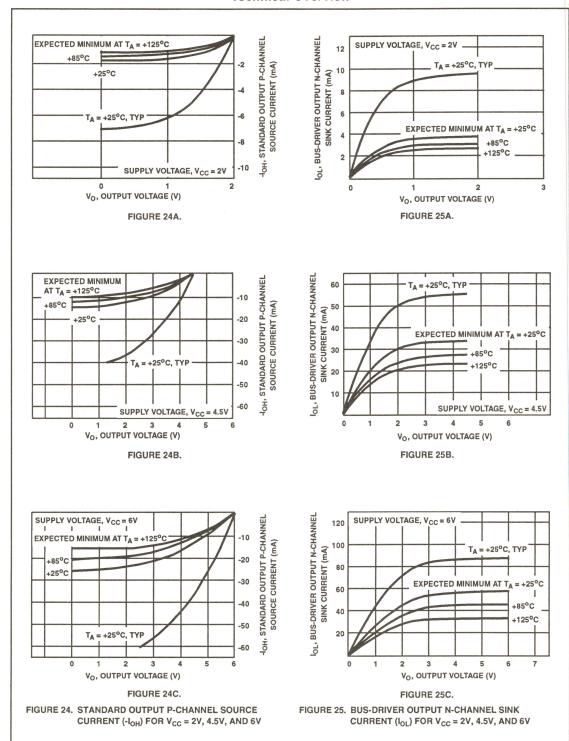
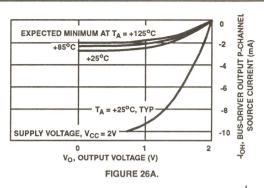
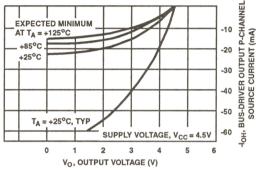


FIGURE 23C.

FIGURE 23. STANDARD OUTPUT N-CHANNEL SINK CURRENT (Io_) FOR V_CC = 2V, 4.5V, AND 6V







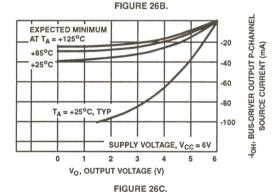


FIGURE 26. BUS-DRIVER OUTPUT P-CHANNEL SOURCE CURRENT (- I_{OH}) FOR V_{CC} = 2V, 4.5V, AND 6V

Dynamic Characteristics

The Harris QMOS family is designed to meet the dynamic switching speeds and operating frequency of low power Schottky TTL. When compared to metal gate CD4000 and 74C series CMOS, QMOS shows a 10 to 1 improvement in AC performance. QMOS types feature balanced propagation delays and transition times specified at conditions similar to LSTTL at a nominal $V_{\rm CC}=5V$ and $C_{\rm L}=15{\rm pF}$, so that the user can relate to the equivalent LSTTL specification. Switching speed limits for QMOS are given at a more realistic $V_{\rm CC}$ of 4.5V and a $C_{\rm L}$ of 50pF. Test waveforms for the HC and HCT types are shown at the end of this section.

Capacitive Load (C_I) Determination

The external capacitive loading (C_L) seen by a QMOS output is required to calculate the propagation delay and operating power dissipation of a logic function. The three components of C_L at a logic node are:

- 1. n C_{IN} where n is the fanout.
- 2. m $C_{\rm OUT}$ where m is the number of three-state outputs on a logic bus.
- C_{STRAY} which is the effective wiring and interconnect capacitance.

$$C_L = n C_{IN} + (m - 1) C_{OUT} + C_{STRAY}$$
 (EQ. 1)

 $C_{\rm IN}$ is shown in Figure 27 for typical HCT and HC type inputs. Note that $C_{\rm IN}$ has peak values at the respective switch points of HCT (1.4V) and HC (2.5V). Capacitance on either side of the peak is a summation of package, lead frame, reverse biased input diode, and CMOS gate-to-source/drain capacitance. The peak capacitance results from the Miller multiplication of C gate-to-drain in the highgain linear transition region. The values of $C_{\rm IN}$ that most typically represent the average loading effect are 4pF for HCT inputs and 3pF for HC inputs. $C_{\rm IN}$ for HCT inputs is higher than that for HC inputs because of the required large gate-to-source/drain capacitance of the large NMOS device widths.

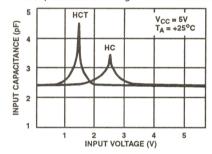


FIGURE 27. CIN AS A FUNCTION OF VIN

Output capacitance (C_{OUT}) is typically 10pF for both HCT and HC-type bus-driver outputs when these versions are in their high-impedance state, the only state where C_{OUT} loading is a factor.

The wiring and interconnect capacitance (C_{STRAY}) is determined by estimates of interconnect capacitance and wiring capacitance. These capacitances are highly variable because of differences in interwiring techniques. An often used high speed wiring technique utilizes strip line with 100Ω characteristic impedance. C_{STRAY} in this case, is typically 20pF per foot. Capacitances of sockets and connectors are available from their manufacturers.

In a bus system, C_{STRAY} is the largest single C_{L} component, as the following example illustrates:

Bus Specification:

No. of fanouts (n) = 10

No. of bus drivers (m) = 5

From Equation 1:

$$C_L = 10 \times 2.5pF + 4 \times 10pF + 7 \times 20pF$$

= 25pF + 40pF + 140pF = 205pF

Propagation Delays vs Supply Voltage

The dynamic performance of a CMOS device is related to its drain characteristics. The drain characteristics are related to the thresholds and gate-to-source voltage potential, $V_{\rm GS}$. The $V_{\rm GS}$ voltage is equal to the power supply voltage, $V_{\rm CC}$. Therefore, a reduction in $V_{\rm CC}$ adversely affects the drain characteristics which, in turn increases the propagation delays. An increase in $V_{\rm CC}$ decreases the propagation delays.

The voltage range of the HCT version is $5V \pm 10\%$. Over this range, the effects of propagation delays on performance are minimal. However, the voltage range recommended for the HC version is 2V to 6V. Over such a wide range, the effects on dynamic performance of propagation delay and operating frequency (Figure 28) are appreciable.

Propagation Delay vs Capacitance

Propagation delay vs capacitance for the Harris family of HC/HCT types is similar to that of LSTTL types which HC/HCT types may replace in present or new applications.

To determine a propagation delay maximum limit at any value of capacitive loading up to 300pF, the following equation is used:

$$t_{PD}(C_L) = t_{PD}(50pF) + t(C_L)[C_L - 50pF]$$
 (EQ. 2)

Where:

t_{PD} (C_L) = maximum propagation delay at the desired C_L

 $t_{PD}(50pF)$ = maximum propagation delay from device data sheet at 2V, 4.5V, or 6V (See Table 5).

 $t(C_L)$ Maximum (ns/pF) multiplying factor from the following table:

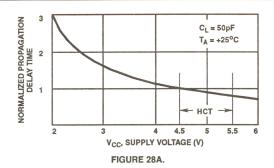
	t(C _L) (ns/pF)					
V _{cc}	STD. OUTPUT	BUS OUTPUT				
2V	0.272	0.187				
4.5V	0.102	0.068				
6V	0.082	0.056				

Propagation Delay vs Temperature

Because an increase in temperature causes a decrease in electron and hole mobilities, a temperature increase will cause an increase in propagation delays. Correspondingly, AC performance improves with lower temperatures. Typically, speeds derate linearly from 25°C at about -0.3%/°C.

The propagation delay, therefore, can be computed at any temperature between -55°C and +125°C by using the following relationship:

$$t_{PD}(T) = t_{PD}(25^{\circ}C) (1 + [(T(^{\circ}C)-25) (0.003ns/^{\circ}C)])$$
 (EQ. 3)



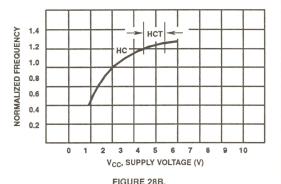


FIGURE 28. TYPICAL SWITCHING SPEED CHARACTERISTIC

Output Transition Times

Table 5 shows the Harris standard and maximum ratings for output transition times applicable to all standard and busdriver outputs. Typical values are approximately 1/2 the maximum values. Practical unspecified minimum values are 1/4 the limit values.

TABLE 5. OUTPUT TRANSITION TIME LIMITS FOR C₁ = 50pF

		MAXIMUM OUTPUT TRANSITION TIMES (ns)				
OUTPUT	V _{CC} (V)	T _A = +25°C	T _A = +85°C	T _A = +125°C		
Standard	2	75	95	110		
	4.5 (Note 1)	15	19	22		
	6	13	16	19		
Bus	2	60	75	90		
Driver	4.5 (Note 1)	12	15	18		
	6	10	13	15		

NOTE:

Specification for CD54HCT and CD74HCT types.

Output Transition Time vs Capacitive Loading

To determine the maximum output transition time on any capacitive loading up to 300pF, the following formula is used:

$$t_{T}(C_{L}) = t_{T}(50pF) + t'(C_{L})[C_{L} - 50pF]$$
 (EQ. 4)

Where:

 $t_T(C_L)$ = Maximum Transition Time at the Desired C_L $t_T(50pF)$ Limit at 2V, 4.5V, or 6V(Table 5)

 $t_TN(C_L) = (ns/pF)$ Multiplying Factor from the Following Table:

	ť(C _L)(ns/pF)				
V _{cc}	STD OUTPUT	BUS OUTPUT			
2V	0.544	0.374			
4.5V	0.204	0.131			
6V	0.170	0.110			

Transition Time vs Temperature

Transition time at HC/HCT outputs typically changes by -0.3%°C. Equation 3 used to compute increase in propagation delay with temperature (see above), can also be used to compute transition time at any temperature by simply substituting t_T for t_{PD} .

Clock Pulse Considerations

All HC/HCT flip-flops and counters contain master-slave devices with level sensitive clock inputs. As the voltage at the clock input reaches the threshold level of the device, data in the master (input) section is transferred to the slave (output) section. The use of voltage threshold levels for clocking is an improvement over AC-coupled clock inputs, however, these levels make these devices somewhat sensitive to clock-edge rates. The threshold level is typically 50% of $\rm V_{CC}$ for HCT devices, and 28% of $\rm V_{CC}$ for HCT devices (1.4V at $\rm V_{CC}=5V$). Temperature has little effect on the clock threshold levels.

When clocking occurs, the internal gates and output circuits of the device dump current to ground. This condition results in a noise transient that is equal to the algebraic sum of internal and external ground plane noise. When a number of loaded outputs change at the same time, it is possible for the chip ground reference level (and therefore, the clock reference level) to rise by as much as 500mV. If the clock input of a positive-edge triggered device is at or near its threshold during a noise transient period, multiple triggering can occur. To prevent this condition, the rise and fall times of the clock inputs should be less than 500ns at $\rm V_{CC}$ 4.5V, the data sheet maximum value.

In the HC/HCT family, several flip-flops have a Schmitt-trigger circuit at their clock input. This circuit increases the maximum permissible rise/fall time on the clock waveform. The Harris flip-flop types HC/HCT 73, 74,107,109 and 112, have special Schmitt-trigger circuits which increase their tolerance to slow rise/fall times and to high levels of ground noise.

Maximum permissible input-clock pulse-frequency ratings on each clocked device type data sheet requires a 50% duty cycle input clock. At these rated frequencies, the outputs will swing rail-to-rail, assuming no DC load on the outputs. This feature is a very conservative and highly reliable method of rating clock-input-frequency limits which for HC/HCT devices, equal or exceed LSTTL ratings.

Power Consumption

The power consumption of a HC/HCT device is composed of two components: one static, the other dynamic. The static component is the result of quiescent current caused principally by reverse junction leakage. The dynamic component results from transient currents required to charge and discharge the capacitive loads on logic elements, that is, transient currents caused by internal and external capacitance, and transients resulting from the overlapping of active p and n transistors. Internal chip power consumption is represented by the value $\mathbf{C}_{\text{PD}}.$

Two equations are used to compute the total IC power consumption. The first, Equation A is applicable to an HC or HCT device when the inputs are driven from GND to V_{CC} (rail-to-rail), as follows:

$$\begin{split} P &= P_{DC} + P_{AC} \\ P &= I_{CC} V_{CC} + C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_O \end{split} \tag{EQ. A}$$

Whore

I_{CC} = Quiescent Current (Ref. Table 6)

V_{CC} = Supply Voltage

f_i = Input Frequency

fo = Output Frequency

C_{PD} = Device Equivalent Capacitance

C₁ = Load Capacitance

The second, Equation B is applicable only to an HCT device where specific input pins are driven at LSTTL levels defined as $V_{\rm IN}$ = $V_{\rm CC}$ - 2.1V:

$$P = P_{DC} + P_{AC}$$

$$P = I_{CC}V_{CC} + \Delta I_{CC}V_{CC}D + C_{PD}V_{CC}^{2}f_{i} + \Sigma C_{L}V_{CC}^{2}f_{O}$$
(EQ. B)

Where:

 Δ I_{CC} = Added DC Current when V_{IN} = V_{CC} - 2.1V (LSTTL level)

D = Duty Cycle of Clock (% of Time HIGH)

TABLE 6. TEMPERATURE - DEPENDENT RATINGS

		LIMIT					
			T _A = +25°C		-40°C TO +85°C	-55°C TO +125°C	
	V _{IN}	v _{cc}	ТҮР	MAX	74HCT MAX	54HCT MAX	UNITS
ΔI _{CC} Additive DC Current Per Input Pin (1-Unit)	V _{CC} - 2.1V	4.5V to 5.5V	100	360	450	490	μА

TABLE 7. HC/HCT AND LSTTL MAXIMUM QUIESCENT CURRENT AT $V_{\rm CC}$ = 5V

	-				
	×				
DEVICE	TYPICAL	LIMIT			LSTTL
COMPLEXITY	25°C	25°C	85°C	125°C	, 125°C
SSI	2nA	2μΑ	20μΑ	40μΑ	4.4mA
FF	4nA	4μΑ	40μΑ	80μΑ	8mA
MSI	8nA	8µА	80μΑ	160μΑ	10mA to 95mA

The temperature dependent ratings for I_{CC} are given in the table below:

HCT LOAD TABL	E BY TYPE SHOWN O	N EACH DATA SHEET
-	Input	Unit Multiplier
Example:	All	X0.6

The dynamic power due to outputs is the sum of the AC power at each output. The user must independently determine the C_L and the average frequency at each output. The latter requires estimating the average frequency of data nodes in a logic system. For example, for HC/HCT counter types, each output is inherently operating at different frequencies.

The source of the C_{PD} or device equivalent-power-dissipation capacitance is made up of 2 sources of internal device power consumption:

- Power consumed by charge and discharge of internal device capacitance.
- 2. Power consumed through current switching transients.

Figure 29 illustrates the typical I_{CC} vs V_{IN} characteristic of HC type devices. Note that when $V_{IN} = 0.1V$ or (V_{CC} -0.1V), zero current flows. Thus, no ΔI_{CC} component is required for computing the power consumption of HC device types. However, the transient switching components of an IC consume power and are a part of the C_{PD} value.

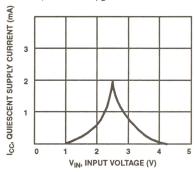


FIGURE 29. I_{CC} vs V_{IN} FOR HARRIS HC TYPES

Figure 30 illustrates the typical I_{CC} vs V_{IN} characteristic of HCT type devices. Again, if input voltages are 0.1V or (V_{CC} -0.1V), no ΔI_{CC} value exists. Also for V_{IN} = 0.4V, ΔI_{CC} is zero. If V_{IN} , however, is an LSTTL logic high level of (V_{CC} -2.1V) or approximately 3V for V_{CC} = 5V, then significant ΔI_{CC} does exit and is indicated in Equation B as the ΔI_{CC} component.

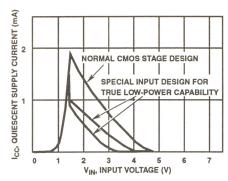


FIGURE 30. I_{CC} vs V_{IN} FOR HCT TYPES

The special input design of Harris HCT types greatly reduces the value of ΔI_{CC} such that the added power is very small; for example, Harris HCT power is minimal compared to LSTTL power. If this special input circuitry were not used, the ΔI_{CC} values would be relatively high as demonstrated by the dashed line in Figure 30, and the HCT type would not have very low power when compared to LSTTL.

NOTE: The low value of I_{CC} is due to a special input design that provides a true low-power HCT capability.

Because appreciable current flows during device input switching as shown in Figure 29 and Figure 30, it is important to maintain fast input rise and fall times. The JEDEC and Harris recommended maximum input rise and fall times are:

1000ns for $V_{CC}=2V$; 500ns for $V_{CC}=4.5V$; 400ns for $V_{CC}=6V$ Since maximum output transition times are 15ns for the standard logic types and 12ns for bus drivers, a designer must only be concerned with exceeding the rise and fall times shown above for interfacing or linear mode operation in applications such as RC oscillators, crystal oscillators, and amplifiers using the HCU04 types.

When Schmitt-trigger types HC/HCT14 and 132 are used for either shaping up slow signals or as RC oscillators, power is increased due to prolonged through-current. For further information on oscillators and their power consumption, refer to Application Note AN7337, "Astable Multivibrator Design Using High Speed QMOS IC's". See Section 8, "How to Use AnswerFAX", of this selection guide.

The adverse effects of power transitions is another reason to maintain input rise and fall times under the recommended limits. Longer transitions may cause oscillations of logic circuits (and hence, logic errors) or premature triggering depending on system V $_{\rm CC}$ and GND noise, which are amplified when input signals hover near the switching voltages illustrated in Figure 29 and Figure 30. To reduce the effects of slower transitions, the use of Schmitt-trigger types is recommended.

Comparison to LSTTL Power

The dynamic power consumption of HC/HCT devices is frequency dependent, but it should be noted that LSTTL power consumption is also frequency dependent at frequencies greater than 1MHz. At frequencies less than 1MHz, the dynamic component is negligible compared to the static

component. The average power consumption of HC/HCT and LSTTL equivalents is illustrated in Figure 31 for four device types. Because all of the functions in a multi-functional LSTTL device are biased when power is applied, the HC/HCT device characteristics are plotted for a single function and for the total package for the purposes of comparison.

Some observations from Figure 31 are:

- For SSI gate types, the HC/HCT power approaches LST-TL power at about 1MHz.
- For higher complexity types such as the Harris HC/ HCT 138 3-of-8 line decoder/demultiplexer shown in Figure 31C, HC/HCT power approaches LSTTL power at above 10MHz.
- 3. Figure 31 implies continuous operation at the frequencies shown, however, most practical applications of logic in microcomputer systems have variable operation or data/ address signal rates. The average operating frequency is much below the peak operating frequency particularly in the 100KHz region where power savings over LSTTL are several orders of magnitude.

Power-Supply Considerations

Power-Supply Voltages

The Harris HC and HCU versions have a power supply range of 2V to 6V; the absolute maximum voltage rating is 7V. The ability to use Harris HC types with a 2V supply makes these devices particularly useful in battery-operated equipment, especially systems including memories that feature 2V standby operation. The absolute maximum supply or ground current, per pin, is ±50mA for types with standard output drive, and ±70mA for types with bus driver outputs.

The operating supply voltage range for Harris CD74HCT types is 4.5V to 5.5V, 5V \pm 10%. These figures indicate that there is more tolerance in the regulation of the low current system supply than is the case with other technologies. The maximum voltage indicated for HC and HCU versions also applies to HCT versions. The advantages of using HC/HCT/HCU with its wider voltage supply range are illustrated in Figure 32.

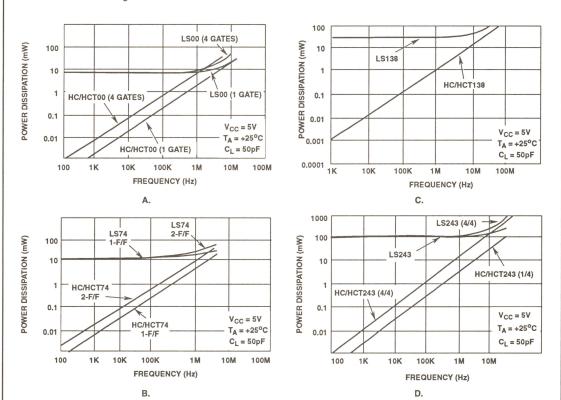


FIGURE 31. POWER vs FREQUENCY GRAPHS FOR (A.) LS/HC/HCT00; (B.) LS/HC/HCT74; (C.) LS/HC/HCT138; (D.) LS/HC/HCT243

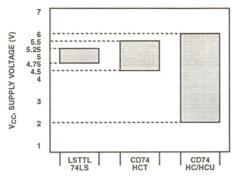


FIGURE 32. POWER SUPPLY RANGES FOR CD74HCT, CD74HC AND CD74HCU VERSIONS OF THE HARRIS FAMILY OF DEVICES AND 74LS SERIES TYPES.

Battery Back-Up

Battery back-up can be easily implemented in systems of Harris HC/HCU devices. An example of this arrangement is shown in Figure 33. The minimum battery voltage required is only 2V plus one diode drop.

In the example, Harris High-to-Low Level Shifters (HC4049 or HC4050) are used to prevent the flow of positive input currents into the system due to input voltage levels greater than one diode drop above $V_{\rm CC}.$ If the circuit design is such that input voltages can exceed $V_{\rm CC},$ then external resistors should be included to limit input currents to 2mA. External resistors may also be necessary in the output circuits to limit currents to 2mA, if the output can be pulled above $V_{\rm CC}$ or below GND. These currents are due to inherent $V_{\rm CC}/{\rm GND}$ diodes that are present in all outputs, including three-state outputs.

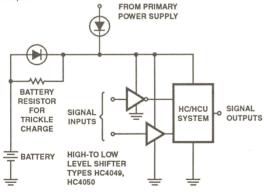


FIGURE 33. EXAMPLE OF AN HC/HCU SYSTEM WITH BATTERY BACK-UP

Power Supply Regulation and Decoupling

The wide power supply range of 2V to 6V may suggest that voltage regulation is not necessary, but it must be realized that a changing supply voltage affects system speed, noise immunity and power consumption. Because noise immunity, and even the correct operation of the circuit, can be affected by noise spikes on the supply lines, therefore, matched decoupling is always necessary in dynamic systems.

Both HC and HCT types have the same power supply regulation and decoupling requirement. The best method of minimizing spiking on the supply lines is by implementing good power supply and ground bussing and having low AC impedances from the V $_{\rm CC}$ and GND pins of each device. Because the minimum value of a decoupling capacitor depends on the voltage spikes that can be allowed, it is a general rule to restrict ground and V $_{\rm CC}$ noise peaks to 400mV. A local voltage regulator on the printed-circuit board can be decoupled using an electrolytic capacitor of $10\mu F$ to $50\mu F$.

Localized decoupling of devices can be provided by a 22nF capacitor for every two to five packages, and a $1\mu F$ tantalum capacitor for every ten packages. The V_{CC} line of bus driver circuits and level sensitive devices can be effectively decoupled from instantaneous loads by a 22nF ceramic capacitor connected as close to the package as possible.

A practical example of determining the value of a decoupling capacitor is as follows: assume that a buffer output sees a 100Ω dynamic load and that the output low-to-high transition is 5V, then the current demand is 50mA per output. For an octal buffer, the current demand would be 0.4A per package, in approximately 6nS.

The following formula can also be used to determine the value of a decoupling capacitor:

The term Q = CV is differentiated to obtain
$$\frac{\Delta Q}{\Delta t}$$
 = $C\frac{\Delta V}{\Delta t}$

Since
$$\frac{\Delta Q}{\Delta t} = I$$
, the equation becomes $I = C \frac{\Delta V}{\Delta t}$

Hence:
$$C = \frac{I\Delta t}{\Delta V}$$

For an octal buffer, assuming a change in V_{CC} or GND of 0.4V then:

$$C = \frac{0.4A \times 6 \times 10^{-9}S}{0.4V} = 6 \times 10^{-9}F = 6nF$$

For further information on power supply regulation and decoupling, refer to Application Note AN7329, "Power-Supply Distribution and Decoupling for QMOS High Speed IC's."

Interfacing

Because of the characteristics of the CMOS output, the HC/ HCT family is very versatile in interfacing between different logic families. This capability including the corresponding fanout is illustrated in Figure 34.

Note that the fanout to CMOS devices is limited only by the input rise and fall times, which are dependent on the capacitive loading, C_L . This dependence can be computed by the following relationship:

$$t_{\rm R}, t_{\rm F} = 2.2 {\rm RC_L}$$
 (EQ. 5)

Where R is the impedance of the output.

$$\begin{array}{c|c} \text{HC/HCT} & \text{TTL, LS, ALS, S} \\ 4000 & \text{74C} & \text{74C} \end{array} \right\} \xrightarrow{\text{TTL, LS, ALS, S}} \\ \text{HCT} \xrightarrow{\text{HCT}} \begin{array}{c} \text{TTL, LS, ALS, S} \\ \text{HC/HCT} \\ 4000 \\ \text{74C} \end{array} \right\}$$

FANOUT FROM	TO (CORRE	ESPON	IDING L	OGIC F	AMILIES
HC/HCT	TTL	LS	ALS	FAST	S/AS	4000, 74C
Standard Types	2	10	20	6	2	See Text
Bus Drivers	3	15	30	10	3	

FIGURE 34. HC/HCT INTERFACING CAPABILITY AND CORRE-SPONDING FANOUT TO OTHER LOGIC FAMILIES

Harris HC types cannot be driven from any of the TTL families because the TTL output voltage high, V_{OH} Min, does not satisfy the HC input voltage high, V_{IH} Min specification. The HCT types can be directly interfaced to the TTL families because the HCT input voltage high, V_{IH} Min is less than the TTL output voltage high, V_{OH} Min. To meet minimum V_{IH} requirements, HC types can use a pull-up resistor as illustrated in Figure 35.

FIGURE 35. USE OF PULL-UP RESISTOR TO INTERFACE TTL AND HC DEVICES.

However, the use of a pull-up resistor will not give optimum performance because as noted in Figure 35, the resistor tends to slow down system speed, increase power dissipation, decrease noise margin, and decrease fanout.

For further information on interfacing, refer to Application Note AN7325, "Interfacing HC/HCT QMOS Logic with Other Families and Various Types of Loads." See Section 8, "How to use AnswerFAX", in this selection guide.

Logic-Level Conversion

The HC/HCT family contains logic-level conversion types necessary to interface high-voltage logic levels (up to 15V common in control and automation systems) to low voltage levels (down to 2V) as shown in Figure 36.

$$V_{CC}$$
 = 2V TO 6V

 V_{IN} = V_{CC} TO 15V AND GND

QMOS HC4049

FIGURE 36A. HEX INVERTING

$$V_{CC} = 2V \text{ TO } 6V$$
 $V_{IN} = V_{CC} \text{ TO } 15V \text{ AND } \text{GND}$

QMOS HC4050

FIGURE 36B. HEX NON-INVERTING
FIGURE. 36. HIGH-TO-LOW LOGIC LEVEL CONVERSION

The Quad open-drain NAND gate (HC/HCT03) is used to convert from HC (2V to 6V) or HCT (TTL or CMOS) logic levels up to 10V output logic levels as shown in Figure 37. $R_{\rm L}$ can be a very wide range of values. For design of this output interface, use the output NMOS transistor characteristics of Figure 23. The minimum value of $R_{\rm L}$ is that necessary to keep the output current below the 25mA HC/HCT family maximum rating. A large value of $R_{\rm L}$ will prolong the output rise time.

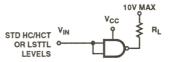


FIGURE 37. LOW-TO-HIGH LOGIC LEVEL CONVERSION

System (Parallel) Clocking

When utilizing the HC/HCT family in synchronously clocked systems the following guidelines should be followed. Because of variations in switching points between devices, a slow clock edge could cause a logic error. If data in one of the synchronously clocked circuits changes before the switching point of the next sequential circuit is reached, a logic error will occur. This situation is illustrated in Figure 38.

V_{S1} = Switching point, Device 1

V_{S2} = Switching point, Device 2

t_P = Propagation Delay

Because of variations in input threshold voltages among Harris HC-version devices, the maximum clock-pulse rise or fall time should adhere to the following relationship:

$$t_{\rm p}$$
, $t_{\rm p} {\rm Max} < 2 t_{\rm p} {\rm Max}$ (EQ. 6)

In a system where HC, HCT, and TTL-type families are mixed, the maximum clock pulse rise or fall times should adhere to the following relationship:

$$t_{\rm R}, t_{\rm F} {\rm Max} < t_{\rm P} {\rm Max}$$
 (EQ. 7)

It is recommended that a Schmitt-trigger circuit be utilized if wave shaping is required.

The maximum rise or fall time into any Harris HC or HCT device must be limited to 1000ns, 500ns, and 400ns at 2V, 4.5V, and 6V, respectively. If these limits are exceeded, noise on the input or power supply may cause the outputs to oscillate during transition. This oscillation could cause logic errors and unnecessary power consumption.

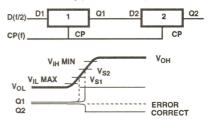


FIGURE 38. RESULT OF CHANGING DATA IN ONE SYNCHO-NOUSLY CLOCKED CIRCUIT BEFORE THE SWITCHING POINT OF THE NEXT SEQUENTIAL CIRCUIT IS REACHED

Drop-In Replacement

The use of Harris HCT family devices make it unnecessary to sacrifice noise margins, speed, and quiescent power dissipation in constructing interfaces to achieve mixed technology designs. This performance is possible because HCT devices are TTL compatible and can directly replace LSTTL counterparts without the addition of pull-up resistors at the LSTTL outputs.

Fanout capabilities should be taken into account when an HCT device is used to replace a TTL part. TTL fanout is usually expressed in unit loads (ULs) and the load is specified to be an input of the same family. In fact, TTL fanout is determined by the ability of the outputs to sink current (a TTL input usually sources current). The outputs of HCT devices are classified in two categories: standard and bus driver. Table 8 shows the fanout for the different TTL families.

For further information on drop-in replacements, refer to Application Note AN7330, "Replacing LSTTL with QMOS High Speed Logic IC's". See Section 8, "How to Use Answer-FAX", in this selection guide.

The fanout values shown in Table 8 are derived at a voltage drop of maximum 0.4V (V_{OL}). In the "74" TTL series, an extended V_{OL} value is often seen, e.g., 8mA at 0.5V voltage drop for LSTTL. If this value is used in determining the fanout of the TTL part, it can result in a higher fanout than is possible with QMOS. This condition can be resolved by replacing as many of the driven TTL parts as possible by HCT devices to reduce the sink current requirement (the HCT input current is negligible). Furthermore, the use of HCT devices results in a substantial reduction in power dissipation.

TABLE 8. FANOUT OF HCT TO TTL ELEMENTS

нст	TTL	LS	ALS	FAST	S AND AS
Standard	2	10	20	6	2
Bus-Driver	3	15	30	10	3

Devices of the HCT family are power saving, virtually drop-in replacements for LSTTL parts. The total power consumed by a system depends largely on the number of gates switching at any time and on the switching frequency, but in most systems only about 30% of all circuits switch at the maximum system frequency; 70% operate at far lower rates. Thus, even in systems using ALS, AS, S and FAST, the HCT family can be used with consequent power savings and good reliability improvement in mixed technology designs.

Conversion of LSTTL Test to HCT Test

A simplified technique to convert an LSTTL test program to one that properly tests an HCT type is explained in Application Note AN7323 "Modification of LSTTL Test Programs to Test HCT High Speed CMOS Logic IC's". See Section 8, "How to use AnswerFAX", in this selection guide.

Bus Systems

Bus systems are commonly used in microcomputer applications. Harris CMOS devices are being increasingly used in these applications. There are several constraints imposed on microprocessor systems in industrial applications, such as electrically noisy environments, battery stand-by requirements and sealed, gas-tight enclosures. QMOS bus systems, e.g., the proposed CMOS STD bus (a non-proprietary CMOS bus proposed standard) provides a low power solution to virtually all of these problems. In comparison with older bipolar digital IC Bus standards, QMOS bus systems offer superior noise immunity, equal operating speed, lower power dissipation, wider supply voltage range, extended temperature range, and enhanced reliability.

In order to optimize results with QMOS, particularly in circuits which communicate directly with the bus, the use of only HC devices is recommended, because HC QMOS optimizes input-signal noise immunity with HC QMOS a new low-power bus termination can be introduced (see Figure 39B) which, unlike the conventional high-current TTL bus termination of Figure 39A, draws no heavy DC current and is more suited to QMOS outputs. Both HC and HCT QMOS have the identical rail-to-rail output drive.

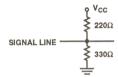


FIGURE 39A. CONVENTIONAL TERMINATIONS FOR TTL BUSES
0.25W PER LINE OR 2W PER OCTAL DRIVE AND
TERMINATION

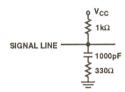


FIGURE 39B. PROPOSED LOW-POWER TERMINATION FOR CMOS STD BUS EQUIVALENTS

FIGURE 39. BUS TERMINATIONS

The wider supply voltage range of HC type QMOS together with its lower power dissipation virtually eliminates problems caused by voltage drops along power buses between cards in a system. It is possible for a circuit to pick up severe noise spikes or differential voltages via the card edge-input protection circuit. Such pick-up can exceed the CMOS input current maximum ratings if the input current is not limited by a $10k\Omega$ series resistor in the QMOS logic line. This series resistor will limit transient current to $\pm 20mA$ for external voltages of up to $\pm 200V$. However, for correct functioning, the DC input current should be kept below 2mA. This type of card edge input protection is shown in Figure 40.

In the circuit of Figure 40, if the input diode current exceeds 2mA, a QMOS high-to-low level shifter should be used (e.g., HC4049, or HC4050).

Because QMOS bus-drivers do not have built-in hysteresis, slowly rising pulses should be avoided or devices with Schmitt-trigger action should be used, such as the QMOS flip-flop series HC/HCT73, 74,107,109,112, or the dedicated Schmitt-trigger types HC/HCT14 and 132. The rise and fall times can be derived from the information given in the section, "Propagation Delays and Transition Times".

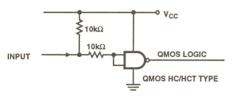


FIGURE 40. EXAMPLE OF THE CARD EDGE-INPUT-PROTEC-TION CIRCUIT

Standardized Capacitance Power Dissipation (C_{PD}) Test Procedure

The purpose of the C_{PD} number is to allow the user to estimate the actual power consumption of his system. Therefore, the table has been set up to exercise each device in the same manner as it would usually be used. Devices which are separable into independent sections are measured on a "per section" basis, the remaining are measured on a "per section" basis. Each part number's unique setup is listed in the Pin Condition Table. The following paragraphs describe the generic set up for each class of devices.

All Part Numbers

Measurements are to be made at $T_A = +25^{\circ}C$, $V_{CC} = 5V$, and three-state outputs both enabled and disabled.

Gates

Switch one input. Bias the remaining inputs such that the output switches.

Latches

Toggle as in a flip-flop.

Flipflops

Switch the clock pin while changing "D" (or biasing "J" and "K") such that the output(s) change each clock cycle. For part numbers with common clocks, exercise the "D", "J", or "K" inputs of only one flip-flop. Set the inputs of the remaining flip-flops so they do not change state.

Decoders/Demultiplexers

Switch one address pin, which changes two outputs.

Data Selectors/Multiplexers

Switch one address input, with the corresponding data inputs at opposite logic levels, so that the output switches.

Counters

Switch the clock pin, with other inputs biased, such that the device counts.

Shift Registers

Switch the clock, adjust the data inputs such that the shift register fills with alternate 1's and 0's.

Transceivers

Switch one data input. For bi-directional transceivers enable only one direction.

Parity Generators

Switch one input.

Priority Encoders

Switch the lowest priority input.

Display Drivers

Switch one input such that approximately half the outputs change state.

ALUs/Adders

Switch one least significant input bit, bias the remaining inputs so that the device is alternately adding 0000 (binary) or 0001 (binary) to 1111 (binary).

Since C_{PD} is a measure of device power consumption, and not that of the driven load, each output would ideally be unloaded. However, this is impractical with automatic testers which often have 30pf to 40pF hanging on each pin. Therefore, each output which is switching should be loaded with the standard 50pF. The equivalent load capacitance, based on the number of outputs switching and their frequency, is then subtracted from the measured gross C_{PD} number to obtain the device's actual C_{PD} value.

If a device is tested at a high enough frequency, static supply current will contribute a negligible amount to power consumption and can be ignored. Thus, it is recommended that power consumption be measured at 1MHz and the following formula be used to calculate C_{PD}:

$$C_{PD} = \frac{(I_{CC})}{(V_{CC})(1E6)} - (Equivalent Load Capacitance)$$

EXPLANATION OF SYMBOLS

Key

- V = V_{CC} (+5V)
- G = Ground
- H = Logic 1 (V_{CC}) Inputs at V_{CC} for HC Types; 3.5V for HCT Types
- L = Logic 0 (Ground)
- D = Don't Care Either H or L But Not Switching
- C = a 50pF Load to Ground
- O = An Open Pin; 50pF to Ground is Allowed
- P = Input Pulse (See Illustration)
- Q = Half Frequency Pulse (See Illustration)
- R = 1k Ω Pull-up Resistor to an Additional 5V Supply Other than the V_{CC} Supply
- B = Both R and C

PIN CONDITION TABLE FOR CPD TESTS

	EQUIV- ALENT													PI	N N	JMB	ER												
HC/HCT TYPES	LOAD (pF)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
00	50	Р	Н	С	D	D	0	G	0	D	D	0	D	D	٧	-	-	-	-	-	-	-	-	-	-	-	-	-	-
02	50	С	Р	L	0	D	D	G	D	D	0	D	D	0	٧	-	-	-	-	-	-	-	-	-	-	-	-	-	-
03	0	Р	Н	В	D	D	0	G	0	D	D	0	D	D	٧	-	-	-	-	-	-	-	-	-	-	-	-	-	-
04	50	Р	С	D	0	D	0	G	0	D	0	D	0	D	٧	-	-	-	-	-	-	-	-	-	-	-	-	-	-
U04	50	Р	С	D	0	D	0	G	0	D	0	D	0	D	٧	-	-	-	-	-	-	-	-	-	-	-	-	-	-
08	50	Р	н	С	D	D	0	G	0	D	D	0	D	D	٧	-	-	-	-	-	-	-	-	-	-	-	-	-	-
10	50	Р	Н	D	D	D	0	G	0	D	D	D	С	Н	٧	-	-	-	-	-	-	-	-	-	-	-	-	-	-
11	50	Р	н	D	D	D	0	G	0	D	D	D	С	Н	٧	-	-	-	-	-		-	-	-	-	-	-	-	-
14	50	Р	С	D	0	D	0	G	0	D	0	D	0	D	٧	-	-	-	-	-	-	-	-	-	-	-	-	-	-
20	50	Р	Н	0	н	н	С	G	0	D	D	0	D	D	٧	-	-	-	-	-	-	-	-	-	-	-	-	-	-
21	50	Р	н	0	н	н	С	G	0	D	D	0	D	D	٧	-	-	-	-	-	-	-	-	-	-	-	-	-	-
27	50	Р	L	D	D	D	0	G	0	D	D	D	С	L	٧	-	-	-	-	-	-	-	-	-	-	-	-	-	-
30	50	Р	Н	Н	н	н	Н	G	С	0	0	Н	Н	0	٧	-	-	-	-	-	-	-	-		-	-	-	-	-
32	50	Р	L	С	D	D	0	G	0	D	D	0	D	D	٧	-	-	-	-	-	-	-	-	-	-	-	-	-	-
42	100	С	С	0	0	0	0	0	G	0	0	0	L	L	L	Р	٧	-	-	-	-	-	-	-	-	-	-	-	-
73	50	Р	Н	Н	٧	D	D	D	0	0	D	G	С	С	Н	-	-	-	-	-		-	-	-	-	-	-	-	-

INPUT PULSES

PIN CONDITION TABLE FOR C_{PD} TESTS (Continued)

	EQUIV- ALENT													PIN	N N	JMB	ER												
HC/HCT TYPES	LOAD (pF)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
74	50	Н	Q	Р	Н	С	С	G	0	0	D	D	D	D	٧	-	-	-	-	-	-	-	-	-	-	-	-		-
75	50	С	Q	D	D	٧	D	D	0	0	0	0	G	Р	0	0	С	-	-	-	-	-	-	-	-	-	-	-	-
85	50	L	Н	Р	Н	0	С	0	G	L	L	L	L	L	L	L	٧	-	-	-	-	-	-	-	-	-	-	-	-
86	50	Р	L	С	D	D	0	G	0	D	D	0	D	D	٧	-		-	-	-	-	-	-	-	-	-	-	-	-
93	47	Q	L	L	D	٧	D	D	С	С	G	С	С	D	Р	-	-	-	-	-	-	-	-	-	-	-	-	-	-
107	50	Н	С	С	Н	0	0	G	D	D	D	D	Р	Н	٧	-	-	-	-	-	-	-	-	-	-	-	-	-	-
109	50	Н	Н	L	Р	Н	С	С	G	0	0	D	D	D	D	D	٧	-	-	-	-	-	-	-	-	-	-	-	-
112	50	Р	Н	Н	Н	С	С	0	G	0	D	D	D	D	D	Н	٧		-	-		-	-	-	-	-	-	-	-
123	100	L	Н	Р	С	0	0	0	G	D	D	D	0	С	0	R	٧		-	-	-	-	-	-	-	-	-	-	-
125	50	L	Р	С	D	D	0	G	0	D	D	0	D	D	٧	-	-	-	-		-	-	-	-	-	-	-	-	-
126	50	Н	Р	С	D	D	0	G	0	D	D	0	D	D	٧	-	-	-	-	-	-	-	-	-	-	-	-	-	-
132	50	Р	Н	С	D	D	0	G	0	D	D	0	D	D	٧	-	-	-	-	-	-	-	-	-	-	-	-	-	-
137	100	Р	L	L	L	L	Н	0	G	0	0	0	0	0	С	С	٧	-	-	-	-	-	-	-	-	-	-	-	-
138	100	Р	L	L	L	L	Н	0	G	0	0	0	0	0	С	С	٧	-	-	-	-	-	-	-	-	-	-	-	-
139	100	L	Р	L	С	С	0	0	G	0	0	0	0	D	D	D	٧	-	-	-	-	-	-	-	-	-	-	-	-
147	50	Н	Н	Н	Н	Н	0	0	G	С	н	Р	Н	Н	0	0	٧	-	-	-	-	-	-	-	-	-	-	-	-
151	100	D	D	L	Н	С	С	L	G	L	L	Р	D	D	D	D	٧	-	-	-	-	-	-	-	-	-	-	-	-
153	50	L	L	D	D	L	Н	С	G	0	D	D	D	D	Р	D	٧	-	-	-	-	-		-	-	-	-	-	-
154	100	С	С	0	0	0	0	0	0	0	0	0	G	0	0	0	0	0	L	L	L	L	L	Р	٧	-	-	-	-
157	50	Р	L	Н	С	L	L	0	G	0	L	L	0	L	L	L	٧	-	-	-	-	-	-	-	-	-	, -	-	-
158	50	Р	L	Н	С	L	L	0	G	0	L	L	0	L	L	L	٧	-	-	-	-	-	-	-	-	-	-	-	-
160	55	Н	Р	D	D	D	D	н	G	Н	н	С	С	С	С	С	٧	-	-	-	-	-	-	-	-	-	-	-	-
161	50	Н	Р	D	D	D	D	Н	G	Н	н	С	С	С	С	С	٧	-	-	-	-	-	-	-	-	-	-	-	-
162	55	Н	Р	D	D	D	D	Н	G	н	Н	С	С	С	С	С	٧	-	-	-	-	-	-	-	-	-	-	-	-
163	50	Н	Р	D	D	D	D	Н	G	Н	Н	С	С	С	С	С	٧	-	-	-	-	-	-	-	-	-	-	-	-

PIN CONDITION TABLE FOR CPD TESTS (Continued)

	EQUIV- ALENT													PI	N NU	IMB	ER												
HC/HCT TYPES	LOAD (pF)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
164	200	Q	Н	С	С	С	С	G	Р	Н	С	С	С	С	٧	-	-	-	-	-	-	-	-	-	-	-	-	-	-
165	50	Н	Р	D	D	D	D	С	G	С	Q	D	D	D	D	L	٧	-	-	-	-	-	-	-	-	-	-	-	-,
166	25	Q	D	D	D	D	L	Р	G	Н	D	D	D	С	D	Н	٧	-	-	-	-	-	-	-	-	-	-	-	-
173	25	L	L	С	0	0	0	Р	G	L	L	D	D	D	Q	L	٧	-	-	-	-	-	-	-	-	-	-	-,	-
174	25	Н	С	Q	D	0	D	0	G	Р	0	D	0	D	D	0	٧	-	-	-	-	-	-	-	-	-	-	-	-
175	50	Н	С	С	Q	D	0	0	G	Р	0	0	D	D	0	0	٧	-	-	-	-	-	-	-	-	-	-	-	-
181	250	Р	Н	Н	L	L	Н	Н	L	С	С	С	G	С	В	С	С	С	L	Н	L	Н	L	Н	٧	-	-	-	-
190	60	D	С	С	L	L	С	С	G	D	D	Н	С	С	Р	D	٧	-	-	-	-	-	-	-	-	-	-	-	-
191	53	D	С	С	L	L	С	С	G	D	D	Н	С	С	Р	D	٧	-	-	-	-	-	-	-	-	-	-	-	-
192	60	D	С	С	Н	Р	С	С	G	D	D	Н	С	С	L	D	٧	-	-	-	-	-	-	-	-	-	-	-	-
193	50	D	С	С	Н	Р	С	С	G	D	D	Н	С	С	L	D	٧	-	-	-	-	-	-	-	-	-	-	-	-
194	100	Н	Q	D	D	D	D	D	G	Н	L	Р	С	С	С	С	V	-	-	-	-	-	-	- 1	-	-	-	-	-
195	125	Н	Н	L	D	D	D	D	G	Н	Р	С	С	С	С	С	٧	-	-	-	-	-	-	-	-	-	-	-	-
221	100	L	Н	Р	С	0	0	0	G	D	D	D	0	С	0	R	٧	-	-	-	-	-	-	-	-	-		-	-
237	100	Р	L	L	L	L	Н	0	G	0	0	0	0	0	С	С	V	-	-	-	-	-	-	-	-	-	-	-	-
238	100	Р	L	L	L	L	Н	0	G	0	0	0	0	0	С	С	٧	-		-		-	-	-		-	-	-	-
240	50	L	Р	0	D	0	D	0	D	0	G	D	0	D	0	D	0	D	С	D	٧	-	-	-	-	-	-	-	-
241	50	L	Р	0	D	0	D	0	D	0	G	D	0	D	0	D	0	D	С	Н	٧	-	-	-	-	-	-	-	-
242	50	L	0	Р	D	D	D	G	0	0	0	С	0	L	٧		-	-	-	-	-	-	-	-	-	-	-	-	-
243	50	L	0	Р	D	D	D	G	0	0	0	С	0	L	٧		-	-	-	-	-	-	-	-	-	-	-	-	-
244	50	L	Р	0	D	0	D	0	D	0	G	D	0	D	0	D	0	D	С	D	٧	-	-	-	-	-		-	-
245	50	Н	Р	D	D	D	D	D	D	D	G	0	0	0	0	0	0	0	С	L	V	-	-	-	-	-	-	-	-
251	100	D	D	L	Н	С	С	L	G	L	L	Р	D	D	D	D	V	-	-	-	-	-	-	-	-	-	-	-	-
253	50	L	L	D	D	L	Н	С	G	0	D	D	D	D	Р	D	V	-	-	-	-	-	-	-	-	-	-	-	-
257	50	Р	L	Н	С	D	D	0	G	0	D	D	0	D	D	L	V	-	-	-	-	-	-	-	-	-	-	-	-

	EQUIV- ALENT													PII	N NL	JMB	ER												
HC/HCT TYPES	LOAD (pF)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
258	50	Р	L	н	С	D	D	0	G	0	D	D	0	D	D	L	٧	-	-	-	-	-	-	-	-	-	-	-	-
259	25	L	L	L	С	0	0	0	G	0	0	0	0	Q	Р	Н	٧	-	-	-	-	-	-	-	-	-	-	-	-
7266	50	Р	L	С	0	Ď	D	G	D	D	0	0	D	D	٧	-	-	-	-	-	-	-	-	-	-	-	-	-	-
273	25	Н	С	Q	D	0	0	D	D	0	G	Р	0	D	D	0	0	D	D	0	٧	-	-	-	-	-	-	-	-
280	100	L	L	0	L	С	С	G	Р	L	L	L	L	L	٧	-	-	-	-	-	-	-	-	-	-	-	-	-	-
283	250	С	Н	L	С	Р	Н	L	G	С	С	Н	L	С	L	н	٧	-	-	-	-	-	-	-	-	-	-	-	-
297	12	Н	Н	Н	Р	Q	L	С	G	D	D	0	0	D	Н	Н	٧	-	-	-	-	-	-	-	-	-	-	-	-
299	250	Н	L	L	С	С	С	С	С	Н	G	Q	Р	С	С	С	С	С	D	L	٧	-	-	-	-	-	-	-	-
354	100	D	D	D	D	D	D	L	Н	L	G	L	L	L	Р	L	L	Н	С	С	٧	-	-	-	-	-	-	-	-
356	50	D	D	D	D	D	D	D	Q	Р	G	L	L	L	L	L	L	н	С	С	٧	-	-	-	-	-	-	-	-
365	50	L	Р	С	D	0	D	0	G	0	D	0	D	0	D	L	٧	-	-	-	-	-	-	-	-	-	-	-	-
366	50	L	Р	С	D	0	D	0	G	0	D	0	D	0	D	L	٧	-	-	-	-	-	-	-	-	-	-	-	-
367	50	L	Р	С	D	0	D	0	G	0	D	0	D	0	D	L	٧	-	-	-	-	-	-	-	-	-	-	-	-
368	50	L	Р	С	D	0	D	0	G	0	D	0	D	0	D	L	٧	-	-	-	-	-	-	-	-	-	-	-	-
373	25	L	С	Q	D	0	0	D	D	0	G	Р	0	D	D	0	0	D	D	0	٧	-	-	-	-	-	-	-	-
374	25	L	С	Q	D	0	0	D	D	0	G	Р	0	D	D	0	0	D	D	0	٧	-	-	-	-	-	-	-	-
377	25	L	С	Q	D	0	0	D	D	0	G	Р	0	D	D	0	0	D	D	0	٧	-	-	-	-	-	-	-	-
390	50	Р	L	С	Q	С	С	С	G	0	0	0	D	0	D	D	٧	-		-	-			-	-	-	-	-	-
393	47	Р	L	С	С	С	С	G	0	0	0	0	D	D	٧	·	-	-	·	-	-		-	-		-	-	-	-
423	100	L	Р	н	С	0	0	0	G	D	D	D	0	С	0	R	٧	-	-	-	-	-	-	-	-	-	-	-	-
533	25	L	С	Q	D	0	0	D	D	0	G	Р	0	D	D	0	0	D	D	0	٧	·		-	-	-		-	-
534	25	L	С	Q	D	0	0	D	D	0	G	Р	0	D	D	0	0	D	D	0	٧		-	-	-	-	-	-	-
540	50	L	Р	D	D	D	D	D	D	D	G	0	0	0	0	0	0	0	С	L	٧	-	-	-	-	-	-	-	-
541	50	L	Р	D	D	D	D	D	D	D	G	0	0	0	0	0	0	0	С	L	٧	-	-	-	-	-	-	-	-
563	25	L	Q	D	D	D	D	D	D	D	G	Р	0	0	0	0	0	0	0	С	٧	-	-	-	-	-	-	-	-

PIN CONDITION TABLE FOR C_{PD} TESTS (Continued)

	EQUIV-													PI	N NL	JMB	ER												
HC/HCT TYPES	LOAD (pF)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
564	25	L	Q	D	D	D	D	D	D	D	G	Р	0	0	0	0	0	0	0	С	٧	-	-	-	-	-	-	-	-
573	25	L	Р	D	D	D	D	D	D	D	G	Н	0	0	0	0	0	0	0	С	٧	-	-	-	-			-	-
574	25	L	Q	D	D	D	D	D	D	D	G	Р	0	0	0	0	0	0	0	C,	٧	-	-	-	-	-	-	-	-
583	250	Н	Н	Н	L	L	С	С	G	С	С	С	Н	Р	L	L	٧	-	-	-	-	-	-	-	-	-	-	-	-
597	25	D	D	D	D	D	D	D	G	С	н	Р	D	Н	Q	D	٧	-		-	-	-	-	-	-	-	-	-	-
640	50	Н	Р	D	D	D	D	D	D	D	G	0	0	0	0	0	0	0	С	L	٧	-	-	-		-		-	-
643	50	Н	Р	D	D	D	D	D	D	D	G	0	0	0	0	0	0	0	С	L	٧	-	-	-		-	-	-	-
646	50	D	L	н	Р	D	D	D	D	D	D	D	G	0	0	0	0	0	0	0	С	L	D	D	٧	-	-	-	-
648	50	D	L	н	Р	D	D	D	D	D	D	D	G	0	0	0	0	0	0	0	С	L	D	D	٧	-	-	-	-
670	100	Q	Q	Q	L	Р	С	С	G	С	С	L	L	L	Р	Q	٧	-	-	-	-	-	-	-	-	-	-	-	-
688	50	L	Р	L	L	L	L	L	L	L	G	L	L	L	L	L	L	L	L	С	٧	-	-	-	-	-	-	-	-
4002	50	С	Р	L	L	L	0	G	0	D	D	D	D	0	V	-						-	-	-	-	-	-	-	-
4015	100	Р	С	0	0	0	D	D	G	D	0	С	С	С	L	Q	٧	-	-	-	-	-	-	-	-	-	-	-	-
4016	0	0	0	0	0	D	D	G	0	0	0	0	D	Р	٧	-		-	-			-	-	-	-	-		-	-
4017	55	С	С	С	С	С	С	С	G	С	С	С	С	L	Р	L	٧	-	-	-	-	-	-	-	-	-	-	-	-
4020	48	С	С	С	С	С	С	С	G	С	Р	L	С	С	С	С	٧	-	-		-	-	-	-	-	-	-	-	-
4024	48	Р	L	С	С	С	С	G	0	С	0	С	С	0	٧		-	-		-	-	-	-	-	-	-	-	-	-
4040	48	С	С	С	С	С	С	С	G	С	Р	L	С	С	С	С	٧			-	-	-			-	-		-	-
4046A	50	0	С	L	0	н	0	0	G	0	0	0	0	0	Р	0	٧	-	-	-	-	-	-	-	-	-		-	-
4049	50	٧	С	Р	0	D	0	D	G	D	0	D	0	0	D	0	0	-		-	-	-	-	-	-	-	-	-	-
4050	50	٧	С	Р	0	D	0	D	G	D	0	D	0	0	D	0	0	-	-	-	-	-	-	-	-	-	-	-	-
4051	0	0	0	0	0	0	L	G	G	L	L	Р	0	0	0	0	٧	-	-	-	-	-	-	-	-	-	-	-	-
4052	0	0	0	0	0	0	L	G	G	L	Р	0	0	0	0	0	٧	-		-	-	-	-	-	-	-		-	-
4053	0	0	0	0	0	0	L	G	G	L	L	Р	0	0	0	0	V	-	-	-	-	-	-	-	-	-		-	-
4059	17	Р	D	Н	L	L	L	L	L	L	L	Н	G	Н	Н	L	L	L	L	L	L	L	L	С	٧			-	-

PIN CONDITION TABLE FOR CPD TESTS (Continued)

	EQUIV- ALENT													PIN	N N	JMB	ER												
HC/HCT TYPES	LOAD (pF)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
4060	106	С	С	С	С	С	С	С	G	С	С	Р	L	С	С	С	٧	-	-	-	-	-	-	-	-	-	-	-	-
4066	0	0	0	0	0	D	D	G	0	0	0	0	D	Р	٧		-	-	-	-	-	-	-	-	-	-	-	-	-
4067	0	0	0	0	0	0	0	0	0	0	Р	L	G	L	L	L	0	0	0	0	0	0	0	0	٧	-	-	-	-
4075	50	Р	L	D	D	D	0	G	L	С	0	D	D	D	٧	-	-	-	-	-	-	-	-	-	-	-		-	-
4094	250	Н	Q	Р	С	С	С	С	G	С	С	С	С	С	С	Н	٧	-	-		-	-	-	-	-	-	-	-	-
4316	0	0	0	0	0	Р	D	L	G	G	0	0	0	0	D	D	٧	-	-	-	-	-	-	-	-	-	-	-	-
4351	0	0	0	0	0	0	0	L	Н	G	G	Н	Р	L	0	L	0	0	0	0	٧	-	-	-	-	-	-	-	-
4352	0	0	0	0	0	0	0	L	Н	G	G	Н	Р	L	0	0	0	0	0	0	٧	-	-	-	-	-	-	-	-
4353	0	0	0	0	0	0	0	L	Н	G	G	Н	Р	L	0	L	0	0	0	0	٧	-	-	-	-	-	-	-	-
4510	55	L	С	D	D	L	С	С	G	L	Н	С	D	D	С	Р	٧	-	-	-	-	-	-	-	-	-	-	-	-
4511	200	L	L	Н	Н	L	L	Р	G	С	С	0	0	С	0	С	٧	-	-	-	-	-	-	-	-	-	-	-	-
4514	100	Н	Р	L	0	0	0	0	0	С	0	С	G	0	0	0	0	0	0	0	0	L	L	L	٧	-	-	-	-
4515	100	Н	Р	L	0	0	0	0	0	С	0	С	G	0	0	0	0	0	0	0	0	L	L	L	V	-	-	-	-
4516	50	L	С	D	D	L	С	С	G	L	Н	С	D	D	С	Р	٧	-	-	-	-	-	-	-	-	-	-	-	-
4518	50	Р	Н	С	С	С	С	L	G	D	D	0	0	0	0	D	٧	-	-	-	-	-	-	-	-		-	-	-
4520	47	Р	Н	С	С	С	С	L	G	D	D	0	0	0	0	D	٧	-	·	-	-	-	-	-	-	-	-	-	-
4538	100	G	R	н	Р	Н	С	С	G	0	0	D	D	L	0	G	٧	-	-	-	-	-		-	-		-	-	-
4543	50	Н	L	L	н	L	Р	L	G	С	С	С	С	С	С	С	٧	-	-	-	-	-	-	-	-	-	-	-	-
7030	325	G	G	С	Р	Q	Q	Q	Q	Q	Q	Q	Q	Q	G	L	С	С	С	С	С	С	С	С	С	С	Р	н	٧
7046A	50	0	С	L	0	Н	0	0	G	0	0	0	0	0	Р	0	٧	-	-	-	·	-	·	ŀ	-	·	-	-	-
40102	5	Р	н	L	L	L	L	L	G	Н	L	L	L	L	С	Н	٧	-	-	-	-	-	-	-	-	-	-	-	-
40103	3	Р	н	L	L	L	L	L	G	Н	L	L	L	L	С	н	٧	-	-	-	-	-	-	-	-	-	-	-	
40104	100	Н	Q	D	D	D	D	D	G	н	L	Р	С	С	С	С	٧	-	-	-	-	-	-	-	-	-	-	-	-
40105	200	L	С	Р	Q	Q	Q	a	G	L	С	С	С	С	С	Р	V	-	-	-	-	-	-	-	-	-	-	-	-

Family Ratings and Specifications‡

Absolute Maximum Ratings

DC Supply Voltage, V _{CC} (Note 1)0.5V to +7.0V DC Input Diode Current, I _{IK}
For V _I < -0.5V or V _I > V _{CC} +0.5V±20mA
DC Output Diode Current, I _{OK}
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$
Standard±25mA
Bus
DC V _{CC} or Ground Current, I _{CC}
Standard±50mA
Bus

Power Dissipation Per Package, P _D
Package E, EN, F, H
$T_A = -55^{\circ}C \text{ to } +100^{\circ}C \dots 500 \text{mW}$
T _A = +100°C to +125°C Derate Linearly at 8mW/°C to 300mW
Package M
T = 55°C to 170°C

Lead Temperature (During Soldering)
At Distance 1/16in. ± 1/32in. (1.59 ± 0.79mm)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Supply Voltage Range (Note 1)
CD54/74HC Types
CD54/74HCT Types
DC Input or Output Voltage, V _I , V _O

 Operating Temperature, T_A
 .55°C to +125°C

 Input Rise and Fall Time, t_R, t_F (Note 2)
 1000ns Max

 at 2V
 1000ns Max

 at 4.5V
 500ns Max

 at 6V
 400ns Max

DC Electrical Specifications - HC Series For CD54HC/CD74HC Types

								;					
						AMBIENT TEMPERATURE, T _A (°C)							
					V _{cc}	+2	5°C	-40°C T	O +85°C	-55°C TO +125°C			
PARAMETERS	SYMBOL	TE	ST CO	NDITIO	NS	(V)	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
High Level Input	V _{IH}					2	1.5	-	1.5	-	1.5	-	٧
Voltage						4.5	3.15	-	3.15	-	3.15	-	٧
						6	4.2	-	4.2	-	4.2	-	٧
Low Level Input	V _{IL}					2	-	0.5	-	0.5	-	0.5	V
Voltage						4.5	-	1.35	-	1.35	-	1.35	V
						6	-	1.8	-	1.8	-	1.8	٧
		V _I I _O											
			STD	BUS	UNIT								
High Level Output	V _{OH} (Note 3)		-20	-20	μА	2	1.9	-	1.9	-	1.9	-	٧
Voltage			-20	-20	μА	4.5	4.4	-	4.4	- "	4.4	-	٧
			-20	-20	μА	6	5.9	-	5.9	-	5.9	-	V
			-4	-6	mA	4.5	3.98		3.84	-	3.7	-	٧
			-5.2	-7.8	mA	6	5.48	-	5.34	-	5.2	-	٧
Low Level Output	V _{OL}	V _{IH} or	20	20	μА	2	-	0.1	-	0.1	-	0.1	V
Voltage		V _{IL}	20	20	μА	4.5	-	0.1	-	0.1	-	0.1	٧
			20	20	μА	6	-	0.1	-	0.1	-	0.1	V
			4	6	mA	4.5	-	0.26	-	0.33	-	0.4	V
			5.2	7.8	mA	6	-	0.26	-	0.33	-	0.4	V

[‡] For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX. See Section 8, "How to use AnswerFAX", in this selection guide.

Family Ratings and Specifications ‡

DC Electrical Specifications - HC Series For CD54HC/CD74HC Types (Continued)

,							CD54HC	/CD74HC	;		
)						
					+25°C		-40°C TO +85°C		-55°C TO +125°C		
PARAMET	ERS	SYMBOL	TEST CONDITIONS	V _{cc} (V)	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Input Leakage I _I (Note		I _I (Note 4)	V _I = V _{CC} or GND	6	-	±0.1	-	±1.0	-	±1.0	μА
		I _{OZ} (Note 5)	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND	6	-	±0.5	-	±5	-	±10	μА
Quiescent	SSI	Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	6	-	2	-	20	-	40	μА
Supply FF			6	-	4	-	40	-	80	μА	
	MSI			6	-	8	-	80	-	160	μА

NOTES:

- 1. Unless otherwise specified, all voltages are referenced to Ground.
- 2. Except Schmitt trigger inputs.
- 3. Not applicable to open drain outputs.
- 4. For digital I/O pins use IOZ limits.
- 5. Also applicable to open drain outputs.

DC Electrical Specifications - HCT Series For CD54HCT/CD74HCT Types

								CD54HCT/CD74HCT					
							AMBIENT TEMPERATURE, T _A (°C)						
											-55°C TO		
						V _{cc}	+25°C		-40°C TO +85°C				
PARAMETERS	SYMBOL	TE	ST CO	NDITIO	NS	(V)	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
High Level Input Voltage	V _{IH}						2.0	-	2.0	-	2.0	-	V
Low Level Input Voltage	V _{IL}						-	0.8	-	0.8	-	0.8	V
V _I				Io									
			STD	BUS	UNIT	1							
High Level	V _{OH}	V _{IH} or	-20	-20	μА	4.5	4.4	-	4.4	-	4.4	-	V
Output Voltage	(Note 1)	V _{IL}	-4	-6	mA	4.5	3.98	-	3.84	-	3.7	-	V
Low Level	V _{OL}	V _{IH} or	20	20	μА	4.5	-	0.1	-	0.1	-	0.1	V
Output Voltage		V _{IL}	4	6	mA	4.5	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I (Note 2)	\	V _I = V _{CC} or GND			5.5	-	±0.1	-	±1.0	- 1	±1.0	μА
Three-State Output Off-State Current	I _{OZ} (Note 3)	V	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND			5.5	-	±0.5	-	±5	-	±10	μА
Quiescent SSI	Icc	V _I =	V _{CC} or	GND, I	0 = 0	5.5	-	2	-	20	-	40	μΑ
Supply FF						5.5	-	4	-	40	-	80	μА
Current MSI						5.5	-	8	-	80	-	160	μА
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4)	Δl _{CC}	V _I = V _{CC} -2.4V			4.5 to 5.5	-	360	-	450	-	490	μА	

NOTES:

- 1. Not applicable to open drain outputs.
- 2. For digital I/O pins use I_{OZ} limits.
- 3. Also applicable to open drain outputs.
- 4. Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

[‡] For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX. See Section 8, "How to use AnswerFAX", in this selection guide.

Family Ratings and Specifications ‡

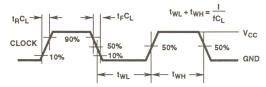
AC Electrical Specifications Definitions

PARA	SYMBOL	MAX	MIN	NOTES	
Propagation Delay	Outputs Going High to Low	t _{PHL}	Х	-	-
	Outputs Going Low to High	t _{PLH}	Х	-	-
Output Transition Time	Outputs Going High to Low	t _{THL}	Х	-	-
	Outputs Going Low to High	t _{TLH}	Х	-	-
Pulse Width	t _{WL} or t _{WH}		Х	1	
Clock Input Frequency	f _{CL}	Х	-	1, 2	
Clock Input Rise and Fall Time		t _{RCL} , t _{FCL}	Х	-	-
Set-Up Time		t _{SU}	-	Х	1
Hold Time		t _H	-	Х	1
Removal Time	Set, Reset, Preset-Enable	t _{REM}	-	Х	1
Three-State Disable Delay Times	High Level to High Impedance	t _{PHZ}	Х	-	-
	High Impedance to Low Level	t _{PZL}	Х	-	-
	Low Level to High Impedance	t _{PLZ}	Х	-	-
	High Impedance to High Level	t _{PZH}	Х	-	-

NOTES:

- 1. By placing a defining Min or Max in front of definition, the limits can change from Min to Max, or vice versa.
- Clock input waveform should have a 50% duty cycle and be such as to cause the Outputs to be switching from 10% V_{CC} to 90% V_{CC} in accordance with the device truth table.

Switching Waveforms for CD54/74HC and CD54/74HCU Integrated Circuits



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 41. CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

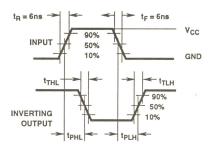


FIGURE 42. TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

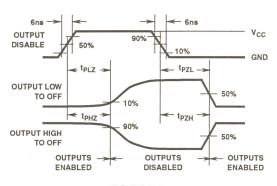


FIGURE 43A.

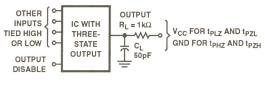
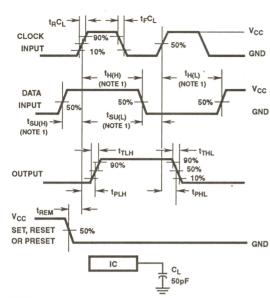


FIGURE 43B.

FIGURE 43. THREE-STATE PROPAGATION DELAY WAVE SHAPES AND TEST CIRCUIT

For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX. See Section 8, "How to use AnswerFAX", in this selection guide.

2-30

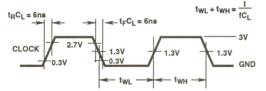


NOTE:

1. (H) or (L) Optional

FIGURE 44. SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND
PROPAGATION DELAY TIMES FOR EDGE
TRIGGERED SEQUENTIAL LOGIC CIRCUITS

Switching Waveforms for CD54/74HCT Integrated Circuits



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 45. CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

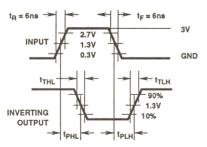
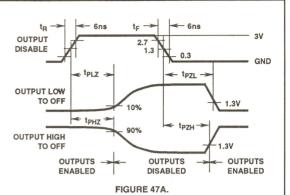


FIGURE 46. TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

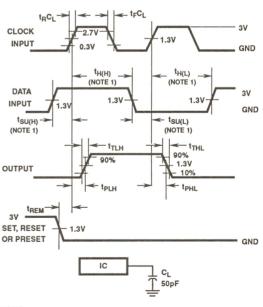


OTHER OUTPUT INPUTS IC WITH $R_L = 1k\Omega$ VCC FOR tPLZ AND tPZL **TIED HIGH** THREE--GND FOR tPHZ AND tPZH OR LOW STATE CL OUTPUT 50pF OUTPUT DISABLE

NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output R_L = 1k Ω to V_{CC} , C_L = 50pF.

FIGURE 47B.

FIGURE 47. THREE-STATE PROPAGATION DELAY WAVE SHAPES AND TEST CIRCUIT



NOTE:

1. (H) or (L) Optional

FIGURE 48. SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIG-GERED SEQUENTIAL LOGIC CIRCUITS

Operating and Handling Considerations

Handling

All inputs and outputs of Harris CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in Application Note, AN6525, AnswerFAX document number 96525, "Guide to Better Handling and Operation of CMOS Integrated Circuits." See Section 8, "How to Use AnswerFAX" of this selection guide.

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{CC} - GND to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{CC} nor less than GND. Input currents must not exceed 20mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or GND, whichever is appropriate.

Output Short Circuits

Shorting of outputs to $V_{\rm CC}$ or GND may damage CMOS devices by exceeding the maximum device dissipation.

Substrate Connection

When these devices (HC or HCT) are used in chip form, as in hybrid applications, the substrate is connected to V_{CC} (as in all N-substrate devices).

PRODUCT FLOW

Enhanced Product

Enhanced Product

The need to achieve the enhanced reliability resulting from burn-in screening must be determined by careful analysis of system design and application.

How many IC's are incorporated into the total system?

How many devices on each board?

Is the proper device being used for the application? What are the reliability goals?

What failure rates are being experienced without screening?

Cost-effectiveness of using enhanced CMOS can be determined by mutual analysis of the economic trade-offs made possible by the following features of the program:

- Available in both plastic and frit-seal ceramic packages.
- · Offered on the industry's broadest line of circuit functions.
- · 0. 025% AQL cumulative.
- · Reduction in PC board reworking through fewer line rejects.
- Lower Warranty Requirements Through the Elimination of Infant Mortality Failures
- Reduced Incoming Inspection Cost by Reduction or Complete Elimination of Test Procedures
- Reduction of System Failures and Related Service Expenses and Customer Complaints

SCREENING DIGITAL ICs (CD TYPES) SUFFIX "X" STANDARD PRODUCT ALL PACKAGES 100% BURN-IN 160 HRS AT +125°C OR EQUIVALENT 100% PARAMETRIC AND FUNCTIONAL TESTS (NOTE1) SAMPLE PARAMETRIC AND **FUNCTIONAL TESTS** AT +25°C AQL = 0.025%(NOTE 1) **ENHANCED PRODUCT** "X" PRODUCT IDENTIFICATION IS BY ADDED SUFFIX "X" TO THE STANDARD BRAND (EXAMPLE: CD74HC00EX) = PRODUCT STATE OR PROCESS = QUALITY ASSURANCE STEP

NOTE:

 For the High Speed CD54/74HC/HCT/HCU products. AC parameters an tested by selecting certain critical propagation delays (which vary from part to part) as indicators of proper AC performance and sample tested to an AQL of 0.025%.

CMOS LOGIC ICS

3

PRODUCT SELECTION GUIDE

ADVANCED CMOS LOGIC - AC/ACT SERIES

	PAGE
TECHNICAL OVERVIEW	3-3
Features	3-3
Input Characteristics.	3-5
Latch-Up Sensitivity	3-8
Output Characteristics	3-9
Dynamic Characteristics	3-15
Power Consumption	3-19
Special Harris AC/ACT Types.	3-22
References	3-22
FAMILY RATINGS AND SPECIFICATIONS‡	3-23
OPERATING AND HANDLING CONSIDERATIONS	3-25
ENHANCED PRODUCT	3-25

For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX. See Section 8, "How to use AnswerFAX", in this selection guide.
3-1

Features

The Harris AC/ACT series of Advanced High Speed CMOS Integrated Circuits is comprised of a broad range of logic types equivalent in performance and speed to FAST, AS (Advanced Schottky), and S (Schottky) bipolar types, but superior in that they require substantially less power in logic operations. Each CMOS circuit function is offered in two basic logic series, as follows:

CD54/74ACTXXX-Series Types. These types feature TTL input-voltage-level compatibility and, using the same standardized pinouts, provide reduced power-consumption alternatives to the very high power consumption of the FAST, AS, and S bipolar logic series types.

CD54/74ACXXX-Series Types. These types feature CMOS input-voltage-level compatibility and, using the same standardized pinouts, provide enhanced system performance (better system noise margin) at speeds similar to those of FAST. AS, and S logic series types.

The AC/ACT family consists of a comprehensive set of octal buffers, octal latches, octal flip-flops, octal transceivers in both the classic 200 series pinout and the newer 500 series flow through pinout. In addition, selected 551 inverters, gates, flip-flops, Schmitt triggers, plus selected MSI counters, registers, multiplexers, decoders and arithmetic functions are included for well over 100 circuits, in both the ACT and AC series

NMOS TRANSISTOR

AC/ACT Family Features

Following is a listing of the features of the AC/ACT family of logic devices.

- Functionally and Pin-Compatible with Industry 54 and 74 Bipolar Types in the FAST, AS, and S Series
- CMOS Rail-To-Rail Output Swing for Maximum Noise Margins
- Fanout (Over Temperature)
 - 2400 AC/ACT Loads
 - 15 FAST Loads
 - 48 AS Loads

NOTE: FAST, AS and S 74 series types are rated for only 0°C to +70°C.

- · Wide Operating Temperature Ranges
 - PDIP and SOIC 74 Series -55°C to +125°C
 - Chip-Form 54 Series -55°C to +125°C
- · Balanced Propagation and Output Transition Times
- Significant Power Reduction Compared to FAST, AS, and S TTL Logic, Resulting In Improved Equipment Reliability
- Outputs Reliably Drive 50Ω Lines (at +85°C) and 75Ω Lines (at +125°C) Without Need for Terminations
- Meets JEDEC Standard Number 20A
- Octal Types Have Typically a 1V Peak (DIP Package) Simultaneous Switching Voltage Transient, Similar to FAST Series.
 Peak is Typically 0.8V in the SOIC Package

PMOS TRANSISTOR

· CMOS Input Compatible

SECOND LEVEL METAL INTERLEVEL DIELECTRIC SILANE FIRST LEVEL METAL OVERCOAT GLASS DASSIVATION GATE 11 mant parted, XXXXX SiO N+ SOURCE N+ DRAIN P+ DRAIN P+ SOURCE N- WELL CHANNEL OXIDE P- IMPLANT P EPITAXIAL LAYER P SUBSTRATE (CONNECTED TO GROUND)

FIGURE 1. CROSS SECTION OF AC/ACT TWO LEVEL METAL CMOS PROCESS

TABLE 1. PERFORMANCE COMPARISON OF AC/ACT AND FAST LOGIC FUNCTIONS

PARAMETERS		SYMBOL	TEST CONDITIONS	74 SE	RIES A	C/ACT	74 S	ERIES F	AST	UNITS
Power Consumption	Power Consumption			POWE	R CONS	SUMPTIO	ON FREC	N FREQUENCY (MHz)		
				0	1	10	0	1	10	
	Four-Stage Counter (191)			0.44	5.5	55	204	224	306	mW
	Octal Transceiver (245)			0.44	39	390	468	514	702	mW
Operating Voltage	FAST				-		4	.75 to 5.3	25	٧
	AC				1.5 to 5.	5		-		٧
	ACT				4.5 to 5.	5		-		٧
Operating Temperatur	e Range			-55 to +125		0 to +70		°C		
Noise Margin	FAST to FAST	V _{CC} = 4.5V, - 0.4/0.3		- 1.25/1.25			٧			
	AC to AC (High/Low)						٧			
	ACT to ACT			1.8/0.36				٧		
Input Switching Voltage Operating Temperature				V _S ± 50		V _S ± 200)	mV	
Output Drive Current	SSI/MSI Logic	l _{OL} /l _{OH}	V _{CC} = 4.5V	±24		±24 +20/-1			mA	
Current	Three-State Buffers				±24			+24/-3		mA
	Bus Drivers				±24			+64/-15		mA
Propagation Delay	Octal Buffer (240)	t _{PHL} /t _{PLH}		7.8/7.8 9.4/9.4				6/9		ns
	Flip-Flop (74)						10.5/8.5		ns	
Input Current		I _{IL}		+1			+1600		μА	
		I _{IH}			-1			-20		μА
Three-State Output Co	urrent				±5			±50		μА

Series Features

Following are the special features of the AC series of Advanced CMOS High Speed ICs.

- 1.5V to 5.5V Operation
- High Noise Immunity
 - $N_{IL} = N_{IH} = 30\%$ for $V_{CC} = 3V$ to 5V
 - $N_{II} = N_{IH} = 20\%$ for $V_{CC} = 1.5V$ to 3V

Following are the special features of the ACT Series of Advanced CMOS High Speed ICs.

- · 4.5V to 5.5V Operation
- · Direct TTL Input Logic Compatible
 - $V_{IL} = 0.8V Max$
 - V_{IH} = 2V Min
- Similar to FAST Specifications Except for the 64mA I_{OL} of FAST Drivers. (See FCT Series of Logic Types for Higher-Current Drivers.)

Comparison of AC/ACT Logic Types with FAST/AS Types

Harris AC and ACT types have many outstanding advantages when compared with the conventional high current bipolar FAST and AS logic types. The Advanced CMOS Logic AC and ACT types can replace the bipolar types in existing equipment and in new equipment designs requiring devices that operate at frequencies up to 100MHz. Table 1 compares the significant operating characteristics of the AC and ACT CMOS types with those of the bipolar FAST logic family.

AC/ACT IC Process and Structure

Advanced CMOS high speed products are fabricated with an advanced small geometry CMOS process and design rules that are tailored to meet the specified high speed and high output drive current, and to tame the high switching current transients associated with high speed designs. Figure 1 shows the cross section of an AC/ACT chip. The starting material is a p-substrate topped with a thin p-epitaxial surface layer; hence, this process is an n-well type. The epitaxial surface serves essentially to eliminate SCR latch up and provides for a low impedance surface conduction path that enhances electrostatic discharge capability. The n and p diffusions are ion-implanted. Polysilicon gates having an effective length of 1.5 µm are deposited over a thin 300Å gate oxide. Active source and drain areas are automatically aligned to the separate gates with the polysilicon gates acting as a mask. This structure drastically reduces the parasitic capacitances between the gate and the n and p areas (see Figure 2) and, as a result, enhances switching speed. The n and p transistors are isolated by the areas of silicon dioxide, as shown in Figure 1.

A major structural feature of AC/ACT devices is the use of two metallization levels. Logic interconnections are shorter because of the dual interconnect layers, and $V_{\rm CC}$ and ground distribution busing is greatly enhanced to handle the switching transient current, which can exceed one ampere for AC/ACT octal buffer types. When used in chip form, the AC/ACT substrate should not be connected to any potential above ground.

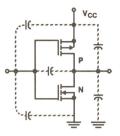


FIGURE 2. PARASITIC CAPACITANCES IN A CMOS INVERTER

Input Characteristics

The inputs of the AC/ACT devices are sensitive to voltage levels. The only input current is the reverse diode leakage (a few picoamperes) of the protection network for electrostatic discharge. The definitive I/O switching characteristics of an input stage is shown in Figure 3 for AC and ACT types. The specified Min/Max input switching voltages are guaranteed over the operating temperature range. Actual shift of the input voltage over the temperature range -55°C to +125°C is 100mV

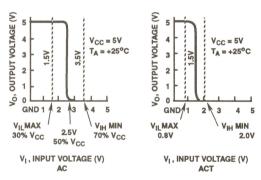


FIGURE 3. AC/ACT I/O SWITCHING CHARACTERISTIC FOR A NOMINAL V_{CC} OF 5V

Noise Immunity and Noise Margin

Table 2 shows the input noise immunity values (VII Max and VIH Min) for AC and ACT devices, the output voltage specifications, and the calculated noise margins under two conditions: (1) interfacing with like members of the same family, and (2) interfacing with bipolar FAST types. The noise margins shown in Table 2A, for AC and ACT types only, apply for the temperature range of -55°C to +125°C. In Table 2B, the interface noise margins are limited to 0°C to +70°C, the commercial temperature range of FAST types. These tables illustrate one of the most important attributes of the CMOS AC/ACT family when compared to the FAST family; namely, designs that use the AC Series CMOS types have over three times the noise margin of the FAST family in the same design. Hence, new designs taking advantage of the higher speeds of these types should use the 1.4V noise margin of the AC family to gain the extra system noise margin of 1V.

Pulsed input noise immunity is illustrated in Figure 4. This figure shows the typical family DC noise immunity for input pulses having widths of 10ns or more. Below 10ns, the pulse amplitude (Vp) reaches higher values before an input is sufficiently disturbed to cause an output change. Note that for AC types, the values are for Vp amplitudes above ground or below VCC (5V). For ACT types, only the limiting noise immunity above ground (0.8V DC) is shown. DC noise immunity below VCC is 3V for ACT types and is not shown here because it is so high.

Input Current/Voltage Characteristic

The inputs of the AC/ACT devices have the dual-diode clamping circuit shown in Figure 5. This circuit serves two important needs: (1) Ringing voltages above V_{CC} and below ground caused by the RLC interface equivalent circuit are clamped to within one diode drop of V_{CC} and ground, thereby reducing EMI. (2) Electrostatic discharge (ESD) is shunted away from the gate oxide of input transistors. Between -0.5V and V_{CC} plus 0.5V (see Figure 6), the input current is typically under the $\pm 1 n A$ typical leakage of the biased input diodes. Beyond -0.5V and V_{CC} plus 0.5V, the diodes are forward biased and clamping action begins. The diodes can handle large junction currents ($\pm 400 m A$ for under one second). For continuous clamping action over the oper-

ating temperature range, the aluminum input metallization traces are reliably sized for ± 20 mA, as shown in Figure 6. Note that it is the aluminum traces and not the diode junctions that are the limiting circuit elements.

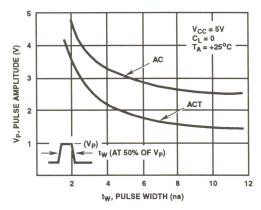


FIGURE 4. TYPICAL DYNAMIC NOISE IMMUNITY

TABLE 2A. NOISE IMMUNITY VALUES AND NOISE MARGIN FOR AC/ACT TYPES (V_{CC} = 5V)

PARAMETERS	SYMBOL	AC TYPES	ACT TYPES	UNITS
Maximum Low-Level Input Voltage	V _{IL} Max	1.5	0.8	٧
Minimum High-Level Input Voltage	V _{IH} Max	3.5	2	٧
Maximum Low-Level Output Voltage	V _{OL} Max	0.1	0.1	V
Minimum High-Level Output Voltage	V _{OH} Min	4.9	4.9	V
Noise Margin Low-Level	V _{NML}	1.4	0.7	V
Noise Margin High-Level	V _{NMH}	1.4	2.9	V

NOTE:

TABLE 2B. NOISE IMMUNITY VALUES AND NOISE MARGIN OF AC/ACT TYPES DRIVING FAST TYPES AND OF FAST TYPES DRIVING AC/ACT TYPES ($V_{CC} = 4.5V$)

PARAMETERS	SYMBOL	AC/ACT → FAST		FAST→	UNITS	
Maximum Low-Level Input Voltage	V _{IL} Max	-	0.8	-	0.8	V
Minimum High-Level Input Voltage	V _{IH} Min	-	2	-	2	٧
Maximum Low-Level Output Voltage	V _{OL} Max	0.44	-	0.5	-	V
Minimum High-Level Output Voltage	V _{OH} Min	3.8	-	2.4	-	V
Noise Margin Low Level	V _{NML}	0.36		0.3		٧
Noise Margin High Level	V _{NMH}	1	.8	0.4		٧

^{1.} $V_{NML} = V_{IL} Max - V_{OL} Max$ $V_{NMH} = V_{OH} Min - V_{IH} Min$

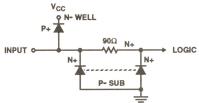


FIGURE 5. AC/ACT DUAL-DIODE INPUT PROTECTION NETWORK

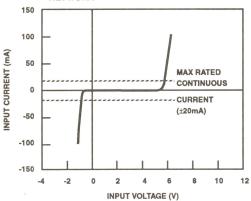


FIGURE 6. AC/ACT INPUT CHARACTERISTIC

Input Termination

The inputs of all AC/ACT types require termination. The input resistance of these types is very high, typically $10^9 \Omega_{\rm A}$ and the input capacitance is a few picofarads. When unterminated inputs are left floating, they can easily pick up stray charge and move the transistor into the linear operating voltage range between $V_{\rm IL}$ and $V_{\rm IH}$. When this transfer takes place, logic malfunction could occur, oscillation may occur, and operating current goes up. Consequently, all unused CMOS inputs must be terminated. Terminations may be directly to $V_{\rm CC}$ or to ground or made by means of a shunt resistor. Specification information on Input Termination Design Rules is located on AnswerFAX, document number 7001, "System Design". See Section 8, "How to Use Answer-FAX" of this selection guide.

Input ESD Protection

As mentioned, AC/ACT device inputs have a resistor-diode protection network, shown in Figure 5, that protects the gate oxide from electrostatic discharge (ESD) damage. The network provides protection to levels greater than 2kV in all modes pertaining to the input, as shown in Figure 7. This 2kV figure was arrived at by the testing of devices in the ESD test circuit shown in Figure 8 while conforming to the MIL-STD test requirements. Despite the excellent built-in ESD protection, these device could be exposed to up to 15kV if good handling practice for semiconductor ICs is not followed. Please refer to AN6525 and ICE 402 for more detailed guidance. One special difference between the Harris AC/ACT logic family and older Harris CMOS families is the use of P

substrates that are at ground potential (see Figure 1). The Harris CD4000B and HC/HCT families of logic devices use N-substrate material, which is at $V_{\rm CC}$ potential. Because of this difference, the bonding sequence for AC/ACT types is changed so that the ground pin is bonded first. The rule for N-substrate logic is to bond the $V_{\rm CC}$ or $V_{\rm DD}$ pad first.

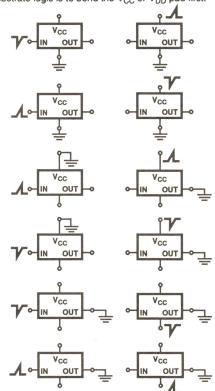
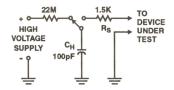


FIGURE 7. ELECTROSTATIC DISCHARGE (ESD) TEST MODES



C_H = HUMAN BODY CAPACITANCE TO GROUND
R_S = BODY SOURCE RESISTANCE

FIGURE 8. TEST CIRCUIT FOR MEASURING ELECTROSTATIC DISCHARGE (ESD) IN AC/ACT CIRCUITS. THE RISE TIME AT THE OUTPUT TERMINAL SHOULD BE 13ns ±2ns

Input Interaction

Another effect of the input protection network is the imposition of a parasitic transistor between adjacent input pins. Figure 9 shows this transistor. This parasitic transistor action may cause undesirable interaction between adjacent inputs

if the input level is less than ground. In AC/ACT devices, gain of the transistor (alpha = $I_{\rm C}/I_{\rm E}$) is minimized to less than 0.001, thereby permitting proper logic operation in the presence of large below ground transient voltages.

An application example in which the knowledge that alpha equals 0.001 is useful is shown in Figure 10. Here, if input A swings between -5V and +5V and the AC/ACT device is operated normally from 5V to ground, it is wanted that the output switch reliably between 0V and 5V. The designer must consider the $V_{\rm ILB}$ at the B input terminal. Calculations show that this is a safe design, because $V_{\rm ILB}$ = 4.3mV.

$$I_{E} = 4.3V/20k\Omega = 0.215\text{mA}$$

$$I_{C} = \alpha I_{E} = 0.215\mu\text{A}$$

$$V_{ILB} = I_{C} \times 20k\Omega = 4.3\text{mV}$$

$$V_{IN} = \text{GND}$$

$$V_{IN} = \text{GND}$$

$$V_{IN} = \frac{1}{100} \times \frac{1$$

FIGURE 9. PARASITIC N-P-N TRANSISTOR BETWEEN ADJA-CENT PINS IMPOSED BY INPUT PROTECTION NETWORK

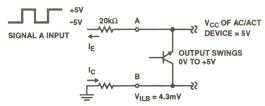


FIGURE 10. EXAMPLE OF USE OF INPUT INTERACTION (A) IN A LEVEL CONVERSION

Input Capacitance

The input capacitance C_l as a function of input voltage is shown in Figure 11 for typical AC and ACT types. Note that C_l has peak values at the respective input-voltage switch point of 1.5V for ACT and 2.5V for AC types. Capacitance on either side of the peak is a summation of package, lead-frame, reverse-biased input diode, and CMOS gate-to source/drain capacitance. The peak capacitance results from the Miller-effect multiplication of the gate-to-drain capacitance in the high-gain linear-transition region. The value of C_l , that most typically represents the average loading effect is 5.0pF for AC and ACT inputs.

Latch-Up Sensitivity

Latch-up is a state in which an unwanted low-impedance path develops in a parasitic four-stage bipolar structure in a CMOS IC. Latch-up may be initiated or triggered by voltage overshoot or undershoot at inputs, outputs, or supply termi-

nals. A high transient voltage or current at any one terminal or at any combination of these terminals may initiate turn on of the parasitic SCR type four-layer diode bipolar device. See Figure 12A.

A simplified diagram of this parasitic structure is shown in Figure 12B. This structure, when triggered on, keeps the supply voltage below the V_{CC} voltage value and thus permits a high supply current of several hundred mA to flow (see IC in Figure 12B). The values of resistors R_P and R_N depend on the circuit layout geometry and on P+ and N+ doping levels. The lower the value of these resistors, the less the voltage drop that will occur and the higher the trigger current needed to induce turn on of the SCR structure.

Also important for minimizing latch-up problems are the established layout rules and process parameters that minimize the current gain (beta) of the parasitic N-P-N and P-N-P transistors shown in Figure 12.

The Harris AC/ACT n-well process uses a thin p-epitaxial layer on the P+ substrate. This layer provides a shunt of very low resistance around $R_{\rm P}$. The effective $R_{\rm P}$ is extremely low, and as a result, very high negative voltage or current transients at the N+ source (V_SS point in Figure 12) are required to forward bias the parasitic N-P-N base-emitter junction. Additionally, there are several design rules that also significantly decrease latch-up probability. These rules relate to:

- Layout spacings to reduce the parasitic N-P-N and P-N-P transistor current gain.
- N+/N- well doping.
- 3. Closed structure outputs.
- 4. Latch plugs liberally used.

The current transient at any input or output terminal that could potentially trigger latch-up of AC/ACT ICs is typically more than ±400mA at +25°C. Measurements are made at all terminals to assure that they have a latch current of over ±100mA at +125°C. The absolute maximum DC rating in AC/ACT data sheets and in the industry JEDEC Standard Number 20A is ±20mA at inputs and ±50mA at outputs.

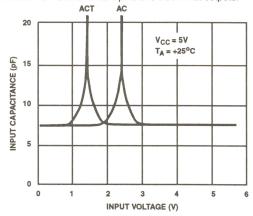


FIGURE 11. VARIATION OF INPUT CAPACITANCE WITH VOLTAGES FOR TYPICAL AC/ACT TYPES

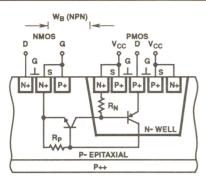


FIGURE 12A. CROSS SECTION OF CMOS STRUCTURE SHOWING SCR LATCH-UP PARASITIC TRANSISTORS

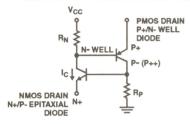


FIGURE 12B. SIMPLIFIED DIAGRAM OF CMOS FOUR-LAYER DIODE STRUCTURE

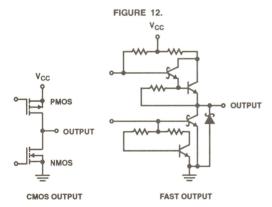


FIGURE 13. AC/ACT OUTPUT, A COMPLEMENTARY-SYMME-TRY TRANSISTOR CONFIGURATION, COMPARED WITH FAST OUTPUT, A TOTEM-POLE CONFIGU-RATION

Output Characteristics

AC/ACT outputs make use of a complementary-symmetry transistor configuration that is different from the FAST totempole output. Both outputs are shown in Figure 13. AC/ACT outputs meet the voltage-level requirements necessary to interface AC/ACT inputs and the drive and current requirements needed to interface bipolar inputs such as TTL, LS, ALS. AS. FAST, and the like.

The outputs of all AC/ACT devices have the same drive current capability and meet proposed JEDEC standard drive and current requirements. The outputs may be active (two-state) or three-state in which both the PMOS and NMOS transistors are off.

Another type of AC/ACT output is the open-drain output of the AC/ACT 05 Hex Inverter shown in Figure 14. The AC/ACT 05 is the only advanced high speed CMOS inverter type having outputs that can be used for a "wired-OR" arrangement. There is, however, a very useful group of octal transceiver types having open-drain outputs. These types are listed below.

AC/ACT 647 Octal Bus Transceiver/Register with Open Drain (Non-Inverting)

AC/ACT 653 Octal Bus Transceiver/Register, Open Drain A Side, Three-State B Side (Inverting)

AC/ACT 654 Octal Bus Transceiver/Register, Open Drain A Side, Three-State B Side (Non-Inverting)

AC/ACT 7623 Octal Bus Transceiver; Three-State B Side, Open Drain A Side (Non-Inverting)

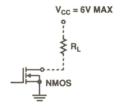


FIGURE 14. AC/ACT HEX INVERTER (05) OPEN-DRAIN OUTPUT CIRCUIT

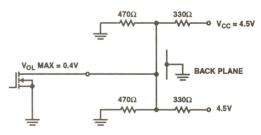


FIGURE 15A. OPEN-DRAIN OUTPUT AC/ACT TYPES EFFEC-TIVELY DRIVE VME

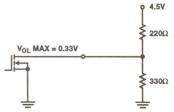


FIGURE 15B OPEN DRAIN AC/ACT TYPES EFFECTIVELY DRIVE SCSI BACKPLANE TERMINATION SCHEMES

FIGURE 15.

These types are especially useful for "wired-OR" -ing of interrupt signals on a backplane. They could also be used for backplane interface using the backplane termination resistors as pull-ups. Figure 15 illustrates two popular backplane termination schemes (VME and SCSI) that are effectively driven with AC/ACT open-drain outputs. In Figure 15A, the dual VME termination scheme is driven, VOL Max is 0.40V at +85°C, and V_{CC} is 4.5V. In Figure 15B, the SCSI termination is driven. In this network, VOL Max is 0.33V. In both examples, the bus pulls up to 2.6V for a VOH Min by means of the resistive terminations. AC/ACT types having three-state outputs may also reliably drive the VME and SCSI termination of Figure 15. With active PMOS pull-ups, the low to high transition of the bus is faster than with the open-drain output interface. See the section on the FCT Bus Interface Family that describes output drives of 64mA and 48mA, required in many backplane applications.

Output ESD Protection

The outputs in AC/ACT devices are protected from electrostatic discharge (ESD) damage by an integral inherent diode structure. Figure 16 shows these diodes. These protective diodes are effective because of the large geometries (widths) of the output transistors. The diodes are comprised of the drain and the n-substrate junction of the p-device and of the drain and the p-well junction of the n-device. This network provides protection to voltage levels greater than 2kV in all electrostatic discharge modes pertaining to the output (for these modes, see Figure 7).

The output clamp diode to V_{CC} must be taken into account in interface and bus applications. For more information on this subject, see AnswerFAX document number 7001, "System Design". See Section 8, "How to Use AnswerFAX" of this selection guide.

Output Current

AC/ACT outputs are specified for both CMOS and bipolar FAST loads. CMOS inputs are voltage sensitive, and the only current is leakage current. The output voltage test for CMOS interfacing is specified for I_O at $\pm 50 \mu A$ (50 CMOS loads). The outputs are also specified for I_O at $\pm 24 \text{mA}$ (15 FAST loads). The corresponding V_{OL} Max and V_{OH} Min for the outputs are given in Table 3.

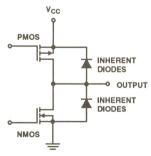


FIGURE 16. INHERENT DIODE STRUCTURE THAT PROTECTS
AC/ACT OUTPUTS FROM ELECTROSTATIC
DISCHARGE DAMAGE TO LEVELS GREATER
THAN 2kV

For output loading of $\pm 50\mu A$, the typical output voltage is only 60mV below V_{CC} or 60mV above ground. As a consequence, CMOS outputs are truly rail-to-rail swings even at $50\mu A$, which is important in many applications. The reason that the guaranteed limits of JEDEC and Table 3 are at 100mV is to facilitate high speed test verification.

Note that for the AC-Series types, operation down to 1.5V is specified. Output current is specified at 1.5V and also at 3V. This worst-case 3V rating is increasingly important because it corresponds to the new low-voltage logic standard (JEDEC Std. No. 8) of 3.3V \pm 0.3V. As CMOS technology shrinks to under one micron, reliability, operating power, and most of all, switching noise all point toward more favorable results with a supply voltage of 3.3V than with 5V ones. At 3.3V, AC/ACT types consume only 40% of the operating power of 5V operation, and switching speed is decreased by an average of only 30%. Also, TTL interface is realizable at 3.3V \pm 0.3V using AC types.

The maximum current per output pin (I_O) is ± 50 mA. This maximum current rating is specified when the outputs (V_O) are in their active regions, that is, greater than ± 0.5 V but less than V_{CC} plus 0.5V. The maximum current rating per power pin, V_{CC} or ground is ± 100 mA for up to four outputs; for each additional output the rating is increased by ± 25 mA. When the output voltage exceeds V_{CC} by more than 500mV or is below ground by more than 500mV, the output protection diodes turn on and conduct current. To avoid latch-up, the peak values of the diode current I_{OK} should not exceed ± 400 mA, as described earlier.

An important contributor to the control of output ringing and electromagnetic interference (EMI) is an output stage design having slow enough output slew rates to allow clamp diode turn-on (about 1ns). This turn-on attenuates ringing that often tries to exceed $V_{\rm CC}$ +0.7V or go more than 0.7V below ground. Control of output slew rates is also a central contributor to reduced output simultaneous switching transients (discussed later).

Output-Current Interfacing Capability

A comparison of the output drive capabilities of AC/ACT types and FAST types follows.

FAST capability is expressed in unit loads (ULs) where the load is specified to be an input of the same family. This specification assures that the worst-case low-input and high-input thresholds will be met and the existing margins of noise immunity preserved.

AC/ACT capability is expressed as source/sink current at a specified output voltage. Because AC/ACT types require virtually no input current, the unit-load concept does not apply.

With a specified output sink current drive of 24mA at 0.44V (at 85°C), each AC/ACT output can drive 24,000 AC/ACT inputs. With a 50 μ A/0.1V specification, each AC/ACT output can drive 480 AC/ACT inputs. Each AC/ACT output has a drive capability of 15 FAST loads and maintains a V_{OL} under 0.5V over the full temperature range.

The standardized Harris and the JEDEC output characteristics are shown in Table 3.

Output Curves

In Figure 17 and Figure 18 the standardized family output characteristic plots are provided. Both typical and worst-case minimum curves plot the $I_{\rm OL}$ (sink) and $I_{\rm OH}$ (source) current as a function of drain-to-source output transistor voltage drop (V_Ds). The heavy line at 50mA is the boundary between safe, continuous operating regions of current drain and areas where only transients are permitted.

Output Short-Circuit Current (Backdriving)

Note that in Figure 17 short-circuit currents of ± 200 mA are typical for AC/ACT outputs at a V_{CC} of 5V. Backdriving these outputs during PC board test by forcing outputs to ground, for example, is permissible with the limitations that only one output per IC be backdriven at any one time and for only one second maximum. For durations longer than one second, the IC may become too hot. Fortunately, because the epitaxial-based process is essentially latch-free, no danger of latch-up results from backdriving.

Output Simultaneous Switching Transients

From Figure 17, it is evident that very large switching transients can be absorbed by AC/ACT output transistors. Figure 19 illustrates how large transient currents are typically generated for the charge or discharge of an AC/ACT output using a 50pF load and a $V_{\rm CC}$ of 5V. The discharge time through the n-device of the output transistor is typically 3ns, even though the capacitor discharge current is typically 83mA, as shown in the following calculation.

$$I_C = C (dv/dt) = 50pF (5V/3ns) = 83mA$$
 (EQ. 1)

The ON resistance of the p and n channels is 10Ω or more each during peak switching transient periods. Thus, it is possible that switching currents of $\pm 200\text{mA}$ per output may occur. For octal types, where bytes are simultaneously switched at common edges, the total peak switching current could approach 8 x 200mA or 1.6 amperes. In practice, however, the actual current is lower because it spreads somewhat as a result of the deviations in peak switching times. These currents cause device V_{CC} and ground bus voltage drops that vary with each output and hence cause different output delays. These delta delays spread the switching current over 1ns to 2ns.

TABLES	STANDARD HARRIS	ANID	IFPEO	OUTDUT	OLIADAO	TEDIOTIOO	AO OFFICE

					T	A, AMBI	ENT TE	MPERAT	URE (°C	C)	
						-0.0		СТО		СТО	
			NDITIONS	V _{CC}		5°C		5°C		5°C	
PARAMETERS	SYMBOL	V _I (V)	I _O (mA)	(V)	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
High-Level Output	V _{OH}	V _{IH} or V _{IL}	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
Voltage			-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05 (Note 4)	4.5	4.4	-	4.4	-	4.4	-	V
			-4	3	2.58	-	2.48	-	2.4	-	V
			-24 (Note 4)	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Notes 1, 2, 4)	5.5	-	-	3.85	-	-	-	V
			-50 (Notes 1, 2, 4)	5.5		-	-	-	3.85	-	V
Low-Level Output	V _{OL}	V _{IH} or V _{IL}	0.05	1.5	-	0.1	-	0.1	-	0.1	V
Voltage			0.05	3	-	0.1		0.1	-	0.1	V
			0.05 (Note 4)	4.5		0.1		0.1		0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
×			24 (Note 4)	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Notes 1, 2, 4)	5.5	-	-	-	1.65	-	-	V
			50 (Notes 1, 2, 4)	5.5			-	-	-	1.65	V

NOTES:

- Test one output at a time for a 1s maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
- 2. Test verifies a minimum 50Ω transmission-line-drive capability at +85°C, 75Ω at +125°C.
- 3. Specifications at 1.5V are not part of the JEDEC proposal.
- 4. For ACT Series, specifications only at V_{CC} = 4.5V and 5.5V apply.

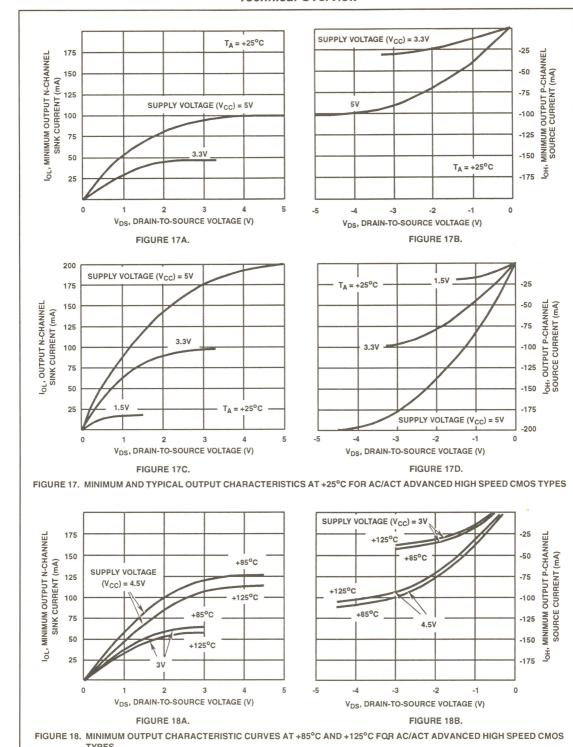


Figure 20 shows that four inductances contribute to the onchip ground potential $V_G.$ These inductances are L1 effective on-chip ground path inductance; L2, the chip bondpad/wire/lead-frame inductance; L3, the IC lead inductance; and L4, the printed-circuit board inductance path to earth or reference ground. Figure 21 illustrates the lifting of ground as a result of the inductances L1 though L4 when an AC/ACT device switches. Instantaneously, the chip sees V_G as ground and causes the following IC performance effects.

- If N outputs switch and one output is a steady-state low, the V_G will reflect onto the unswitched output as the peak low-level output voltage V_{OLP}, as shown in Figure 22B for an eight-output device.
- The instantaneous gate-to-source voltage decreases by a magnitude of V_G volts. This decrease reduces the transistor g_m, raises the R_{ON}, and increases the transition time of the output stage and the delay time.
- Input noise immunity is instantaneously decreased by V_G volts, and as a result, internally stored data in latches or flip-flops could be upset.

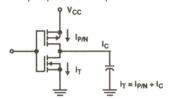


FIGURE 19. GENERATION OF LARGE TRANSIENT CURRENTS FOR CHARGE OR DISCHARGE OF AN AC/ACT OUTPUT. LOAD = 50pF; V_{CC} = 5V

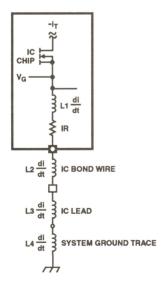


FIGURE 20. IC GOUND PATH AND FOUR CONTRIBUTING INDUCTANCES

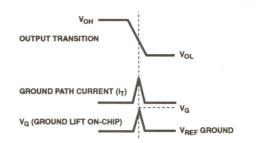


FIGURE 21. GROUND LIFT CAUSED BY SWITCHING CURRENT TRANSIENTS THROUGH INDUCTANCES DESCRIBED IN FIGURE 20

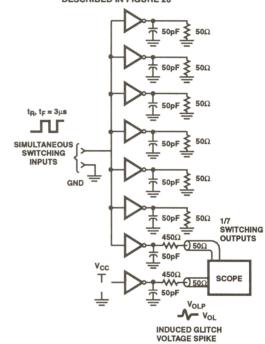


FIGURE 22A. TEST CIRCUIT OF SIMULTANEOUS SWITCHING TRANSIENT

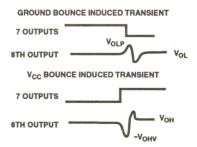


FIGURE 22B. WAVEFORM OF SIMULTANEOUS SWITCHING TRANSIENT

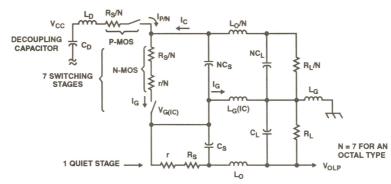


FIGURE 23. EQUIVALENT CIRCUIT OF GROUND-BOUNCE CONFIGURATION FOR AN OCTAL OUTPUT STAGE. DYNAMIC VALUE OF R_S AND TRANSISTOR SWITCH TIMING ARE KEY VARIABLES IN MINIMIZING GROUND BOUNCE (V_{OLP})

Figure 23 shows the equivalent IC circuit for the octal-type ground-bounce test configuration. Although this circuit shows the several RLC components involved in the development of both the transient ground lift (V_G) and the resultant quiet output voltage bounce (V_{OLP}), some key variables that complicate analysis are not readily apparent. These variables include:

- Design of transistors to increase effective R_S, which will increase turn-on time or output slew rate dv/dt. The actual value of R_S is about 15Ω.
- Design of chip to equalize the on-chip L and R of all eight output-stage metal runs to ground.
- Design of the plastic package lead-frame to reduce the ground pin inductance L_G by one half. For the DIP package this inductance is 7.5nH.
- Design of small break-before-make capability to reduce I_{P/N} through current. Time difference is a nominal 0.5ns.
- 5. Design of transistor turn-on time of a nominal 0.75ns.

Of these five variables, the vast majority of ground-bounce minimization is achieved by control of the output dv/dt. It is of so little benefit to change the position of the ground pin or add additional ground pins that users get excellent performance and minimization of ground bounce and EMI without incurring significant extra cost and the reduced reliability of bigger packages that would result from such changes.

Sample Measurement of VOLP

Figure 24 shows actual sample measurement values of the peak low-level output voltage $V_{\rm OLP}$ measured on an ACT240, an Octal-Buffer Line Driver, three-state device. The worst-case $V_{\rm OLP}$, 1.06V, occurs at pin 18, which is furthest from pin 10 ground. The best-case $V_{\rm OLP}$, 0.720V, occurs at pin 9, closest to pin 10. Waveforms for the ACT240 in the dual-in-line package (DIP) are given in Figure 25 and in the small outline package (SOP) in Figure 26. These waveforms are measured at pin 18, the worst-case pin. All Harris octals now have controlled output edge rates with ground-bounce performance similar to that shown in Figure 25 and Figure 26.

This performance is very reasonable for a buffer having a typical delay of 3.5ns. Harris advanced high speed CMOS octal logic devices have been designed to minimize the effective on-chip L1 (Figure 20) and also to minimize L2, the dual bond-wire inductance. L3 is the inductance of a "cornerpin" dual-in-line (DIP) or small outline (SOP) package, and L4 is the inductance of the fixture ground-return path. This last value must be kept small (see next section on $\rm V_{\rm OLP}$ Measurement Method). For comparison, a bipolar FAST F240 type was identically measured. Its $\rm V_{\rm OLP}$ is nearly identical, the worst-case value being 1.05V.

Type	: AC240
	Worst-Case Value
	Best-Case Value 0.72V DIP
	Worst-Case Value 0.75V SOP

FIGURE 24. MEASURED VALUES OF V_{OLP} MADE ON A 240 OCTAL BUFFER LINE DRIVER, THREE-STATE DEVICE

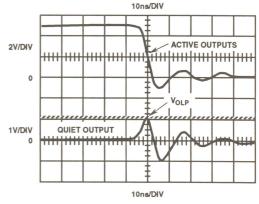


FIGURE 25. SIMULTANEOUS SWITCHING TRANSIENT PER-FORMANCE OF AN AC240 OCTAL-TYPE IC IN A DUAL-IN-LINE (DIP) PACKAGE. SEE FIGURE 22 FOR TEST CONDITIONS

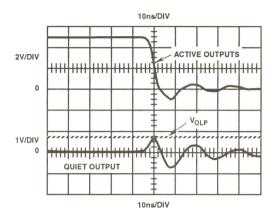


FIGURE 26. SIMULTANEOUS SWITCHING TRANSIENT PERFORMANCE OF AN AC240 OCTAL-TYPE IC IN A SMALL-OUTLINE (SOP) PACKAGE. SEE FIGURE 22 FOR TEST CONDITIONS

VOLP Measurement Method

The method for measuring V_{OLP} , also referred to as the simultaneous switching transient or ground-bounce effect, is a radio-frequency-type measurement and requires a good rf quality test fixture. A schematic of the fixture is given in Figure 22A. It utilizes seven outputs switching into a standard AC/ACT load, considered to be a worst-case condition. The eighth input is held low or high, thereby placing the output in a high or low state. The eighth output is monitored with a scope, and the peak amplitude of the positive transient (V_{OLP}) above V_{OL} is measured. The peak amplitude of the negative transient below V_{OH} is V_{OHV} Figure 22B shows the waveforms of the ground-bounce-induced transients, both positive and negative.

The major concern of the design engineer in making these measurements is the $V_{\rm OLP}$. Tolerance of this unwanted noise voltage is highly dependent on the switching threshold and noise margin of the logic circuits connected to the outputs of the device. With the CMOS switching threshold, which is typically 50% of $V_{\rm CC}$, the energy of the transient pulse is usually insufficient to cause false switching. More critical is when the logic inputs connected to the device switch at TTL thresholds, typically 1.5V.

Dynamic Characteristics

Switching Speed

Significant speed improvement distinguishes the new AC/ACT Advanced High Speed CMOS Logic Family from the HC/HCT High Speed CMOS Logic Family. Table 4 positions each CMOS logic family with the speed-equivalent TTL family. From the standpoint of speed, the AC/ACT family substitutes very adequately for the TTL FAST, AS, and S families. It is not recommended, however, to directly substitute AC/ACT, FAST, AS, S, or ALS logic for HC/HCT or LSTTL logic because of the three times faster switching edges of the former group compared to the latter. These faster families

require transmission-line interconnect considerations, terminations, superior decoupling, and careful PC board layout to keep switching noise generation under control so that FCC emission specifications may be met with good margin.

TABLE 4. GUIDE FOR SUBSTITUTING CMOS LOGIC FAMILY TYPES FOR TTL FAMILIES

CMOS	TTL FAMILY						
LOGIC FAMILY	TTL	LSTTL	ALS	S	FAST	AS	
HC/HCT	Х	Х	X (Note 1)	-	-	-	
AC/ACT	(Note 2)	(Note 2)	X (Note 2)	Х	Х	Х	

NOTES:

- HC/HCT substitutes when ALS is used vs LS for lower power. AC/ ACT substitutes when ALS is used vs LS for higher speed.
- 2. There is too large a difference in speed and noise/EMI generation for AC/ACT to reliably substitute for TTL, LSTTL, or HC/HCT.

Propagation Delays

The useful speed of a logic family is essentially the I/O propagation delay of both low-to-high and high-to-low signal transitions from input to output.

Table 5 provides a comparison of AC and bipolar FAST device propagation delays for three familiar logic types; namely, a NAND gate (00), a flip-flop (74), and an octal buffer (240). Also shown is the input clock rate. For 74-series devices, the delays and also the clock rate are very nearly the same, not withstanding that for AC types V_{CC} is 4.5V and T_A is +85°C and for FAST types V_{CC} is 4.75V and T_A is +70°C. These test conditions are clearly in favor of FAST by about 5%. Also evident from the data sheet extractions in Table 5 are the balanced delay of AC types and the unbalanced (t_{PL} H vs t_{PHL}) delay of the bipolar types.

TABLE 5. COMPARISON OF SWITCHING SPEED FOR THREE 74-SERIES AC AND FAST LOGIC FUNCTIONS

PRODUCT	PARAMETER	AC	FAST	UNIT
Two-Input NAND (00)	t _{PLH} /t _{PHL}	6.2	6/5.3	ns
Flip-Flop (74)	t _{PLH} /t _{PHL}	9	7.8/9.2	ns
	f _{MAX}	125	100	MHz
Buffer (240)	t _{PLH} /t _{PHL}	6.5	8/5.7	ns

Useful delay is only as good as the worst or slowest delay mode or path. For the entire AC/ACT family covering over 50 different logic functions, the speed comparison illustrated in Table 5 holds up within a window of plus or minus a few nanoseconds. There are, however, a few exceptions going in both directions. Where speed right up to the limit of the device capability is a critical design element, the designer should precisely use published data sheet limits for either AC/ACT or FAST types. Table 6A lists three ACT types in which two extra buffer stages are designed in to reduce the incremental change in I_{CC} caused by switching of the input state at 1.5V instead of 2.5V, the optimum value for CMOS devices.

As shown in Table 6B, the 6ns delay of the AC04 Hex Inverter type matches the delay of FAST types. The two extra ACT buffer stages, however, extend the delay limit to 8.8ns. These three SSI types are the only ones having extra ACT stages, and hence, their delay limits are a few nanoseconds slower than those of their AC or FAST counterparts.

TABLE 6A. DEVICES HAVING EXTRA STAGES FOR REDUCING POWER CONSUMPTION

	NUMBER OF LOGIC STAGES		
TYPE	AC	ACT	
04/05 Hex Inverter	3	5	
00 Quad Two-Input NAND	3	5	
86 Quad Two-Input Exclusive-OR	4	5	

TABLE 6B. PROPAGATION DELAY AND ΔI_{CC} VALUES FOR HEX INVERTER TYPE 04

PARAMETER	AC	ACT	FAST	UNIT
t _{PLH} /t _{PHL}	6/6	8.8/8.8	6/5.3	ns
Δl _{CC} per Input	-	0.5 (Note 1)	-	mA

NOTE:

 For three stages instead of five this value would be about 3mA per input.

Data sheets give a finite number of specified values of switching speed at specific test conditions. The system design engineer, however, often needs to know speed limits at other conditions. For example, the propagation delay of a 74 dual D-type flip-flop clock to Q/\overline{Q} is specified as:

$$t_{PLH}$$
, $t_{PHL} = 9.1$ ns Max, $V_{CC} = 4.5$ V, $T_{A} = +85$ °C = 2.65ns Min, $V_{CC} = 5.5$ V, $T_{A} = -40$ °C

There are two dichotomies: (1) The PCB V_{CC} value is fixed at a given time, probably close to 5.0V, and (2) the temperature is fixed at a given time, probably close to 55°C. Thus, the 9.1ns to 2.65ns spread, shown above, is unrealistically large. To ease this problem, Figure 27 is provided. Using this set of normalized delay curves, the system designer can easily narrow the Min/Max delay for use in estimating system timing. For the 74 dual D-type flip-flop if operation is assumed at $V_{CC}=5.0$ V, and $T_A=55$ °C, the Min/Max delay spread is narrower.

$$t_{PLH}$$
, $t_{PHL} = 8.3$ ns Max
= 3.6ns Mln

Use of Figure 27 is as follows:

- 1. Select the maximum delay from the device data sheet for $V_{\rm CC}=4.5V,\,T_A=+125^{\circ}C.$ Call this value X.
- Multiply X by the normalized multiplier fractions of X shown on the vertical axis for a given value of V_{CC} and temperature.

Each AC/ACT data sheet now contains speed limits at two temperature ranges for commercial/industrial plastic packaged product. These ranges are -40°C to +85°C and -55°C to +125°C. The latter temperature range limits are also applicable to MIL product packaged in ceramic packages. Historically, commercial TTL logic types use a limited temperature range for plastic (74 series) of 0°C to +70°C. To readily determine Harris AC/ACT speed for 0°C to 70°C operation, the following multipliers (from Figure 27) are used:

Max Limit = 0.855 X,
$$T_A$$
 = 70°C, V_{CC} = 4.75V Min Limit = 0.25 X, T_A = 0°C, V_{CC} = 5.25V

Where X is the Max Data Sheet limit for $\rm T_A = +125^oC,\ V_{CC} = 4.5V.$

Also shown in Figure 27 is the typical curve of speed vs temperature for V_{CC} = 5V. The exact value at T_A = +25°C is 0.487 X.

Propagation Delay Performance Curves

Figure 28 shows the typical normalized propagation delay as a function of capacitance loading at supply voltages of 1.5V, 3.3V, and 5V. The reference load is 50pF, the rated value given in the device data sheet. Figure 29 shows the typical normalized propagation delay as a function of supply voltage. This curve shows that AC-Series types are typically 30% slower at 3.3V than at the referenced 5V. At a supply voltage of 1.5V, the speed is four times slower compared to the speed at 5V but still is quite fast. In Figure 30, the normalized AC/ACT propagation delay variation with chip operating ambient temperature is given for operation at 1.5V, 3.3V, and 5V. From the 5V curve, it can be concluded that AC/ACT types slow down by 0.3% per °C, a useful number to have available for reference.

Behavioral Models

Behavioral models for Harris AC/ACT types are available from Logic Automation, Inc. These models contain the Min/Max speed limits specified in the Harris data sheets. See AnswerFAX document 7002, "Behavioral Models". See Section 8, "How to Use AnswerFAX" of this selection guide.

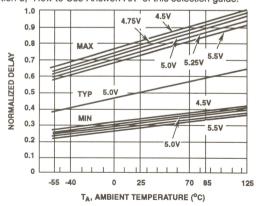


FIGURE 27. NORMALIZED AC/ACT MIN/MAX DELAY AS A FUNC-TION OF SUPPLY VOLTAGE AND TEMPERATURE

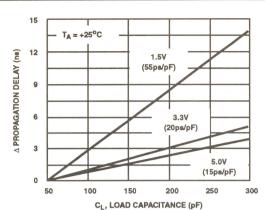


FIGURE 28. TYPICAL CHANGE IN PROPAGATION DELAY AS A FUNCTION OF LOAD CAPACITANCE FOR AC/ACT TYPES

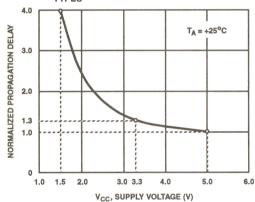


FIGURE 29. NORMALIZED PROPAGATION DELAY AS A FUNC-TION OF SUPPLY VOLTAGE FOR AC TYPES

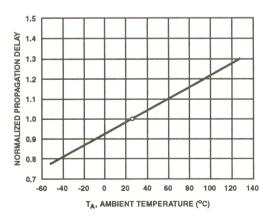


FIGURE 30. NORMALIZED PROPAGATION DELAY AS A FUNC-TION OF AMBIENT TEMPERATURE FOR AC/ACT TYPES

Output Edge Rates/Transition Times

The typical propagation delay of an AC/ACT gate or buffer is 3.5ns (at V_{CC} = 5V, T_A = +25°C, C_L = 50pF), and the high speed of all AC/ACT types necessitates quick and predictable output transition times. Typical AC/ACT output transition times are shown in Table 7. Note that octal types have longer output transition times so as to reduce simultaneous switching transients and ringing.

TABLE 7. TYPICAL OUTPUT TRANSITION TIME (t_{TLH} , t_{THL}). MEASURED BETWEEN THE 10% AND 90% TRANSITION POINTS. $T_A=+25^{\circ}C$

		TYPICAL t _{THL} , t _{TLH} (ns)		
C _L (pF)	V _{CC} (V)	LOGIC	OCTAL	
50	1.5	8	10	
	3.3	3	4	
	5	2.5	3.3	
150	1.5	20	26	
	3.3	8	10	
	5	6	8	
300	1.5	35	46	
	3.3	11	15	
	5	10	13	

Fortunately, unlike bipolar FAST logic, the design engineer may insert series resistors (R_S) in the output circuit, as shown in Figure 31, to reduce the spectral content, dampen ringing, and act as a series terminator. Propagation delay, however, will increase as a result of the series resistor and the associated total shunt capacitance C_S . For CMOS loads, an R_S , even up to several $k\Omega$ in value, will not affect input switching because the input resistance (R_I) is greater than $1000M\Omega$. For bipolar FAST devices, however, adding a series resistor results in increased values of V_{IL} because I_{IL} is 1.6mA. Hence, 100Ω is probably the maximum value for R_S with FAST ICs. This topic is covered in more detail in AnswerFAX document number 7001, "System Design". See Section 8 "How to Use AnswerFAX" of this selection guide.

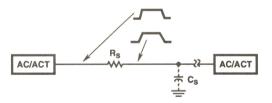


FIGURE 31. USE OF SERIES TERMINATION RESISTOR TO IN-CREASE OUTPUT EDGE RATES

Three-State Ratings and Test Conditions

AC/ACT logic types that have three-state output stage design also have the necessary three-state propagation delay parameters that are uniquely tested to optimize AC/ACT performance. Figure 32A shows an 85°C equivalent ac test circuit for all propagation delay parameters. The three "Thevininized" loads show the load board configuration for testing the six applicable delay parameters. In Figure 32B,

the active-to-high-impedance test waveforms are shown. Take particular notice of the RC symmetry for t_{PLZ} and t_{PHZ} , which is specially suited to CMOS rail-to-rail outputs with switching at 50% of V_{CC} (AC family). Also, note that the test switch point is at 20% of the rail - not 10%. The reason for this increase is that 10% of 4.5V would leave practically no room for the test set comparator because the 250 Ω load pulls rails close to 10% of 4.5V.

There are two factors that must be highlighted:

- 1. The t_{PHZ} test load is different from the FAST test load. For FAST, R is 500Ω for t_{PHZ} and 250Ω for t_{PLZ} . These test loads are very satisfactory for the bipolar totem-pole output offset to 1.5V for V_S and a limited swing of 3V to 4V, but the unbalanced loads are unsatisfactory for AC/ACT outputs.
- FAST test points are at 10% of the output swing, not 20%. Because of this difference, AC/ACT t_{PHZ} and t_{PLZ} parameters are specified a few nanoseconds larger than for FAST types. This change gives the appearance that AC/ACT types are slower than FAST types, but in actual operation, they are very comparable.

Incremental Propagation Delay Caused by Simultaneous Switching

Table 8 illustrates the effects of ground and V_{CC} "bounce" resulting from the simultaneous switching of eight Octal Buffer outputs. Note that the incremental delay added to t_{PHL} is less than that added to t_{PLH} . The reason for this difference is that the Harris chip design and the design of the bond-pad-to-lead frame are geared heavily to reducing the very critical ground loop inductance because of the 0.8V V_{IL} of ACT and FAST inputs. On the high side, where V_{IH} is 2V and the loaded V_{OH} is 3.8V, the V_{CC} bounce is not so critical. Also shown in Table 8 is the shift in skew due to V_{CC} and ground-bounce effects. The cause of these effects is described earlier in this Manual starting under the heading Output Simultaneous Switching Transients.

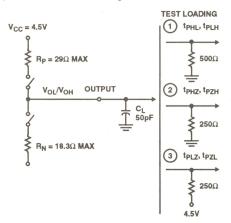


FIGURE 32A. AC/ACT THREE-STATE TEST CIRCUIT. OUTPUT STAGE AND THE THREE JEDEC AND HARRIS TEST LOAD CIRCUITS, $T_A = +85^{\circ}C$

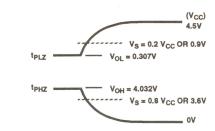


FIGURE 32B. THREE-STATE OUTPUT WAVEFORMS AND TEST POINTS. THE RC TIME CONSTANT IS A BALANCED 250 Ω AND 50pF

FIGURE 32.

TABLE 8. INCREMENTAL PROPAGATION DELAY OF AN AC244 OCTAL NON-INVERTING BUFFER TYPE

	NUMBER OF OUTPUTS SWITCHING		
TEST CONDITIONS	1 (BEST)	8 (WORST)	
$V_{CC} = 5V; C_L = 50pF; T_A = +25^{\circ}C$	(DE31)	(WORST)	
Buffer Measured			
Input Pin	2	2	
		(Note 1)	
Output Pin	18	18	
Data (ns)			
t _{PLH}	4.9	6.41	
t _{PHL}	4.88	6.04	
Incremental Delay (ns) Referred To One Buffer Switching			
t _{PLH}	0	+1.51	
t _{PHL}	0	+1.16	
Skew Of t _{PHL} /t _{PLH} Ratio	0.996	0.942	

NOTE

Clock Pulse Considerations

All AC/ACT flip-flops and counters contain master-slave devices having level-sensitive clock inputs. As the voltage at the clock input reaches the threshold level of the device, data in the master (input) section is transferred to the slave (output) section. The use of threshold levels for clocking is an improvement over ac-coupled clock inputs. These levels, however, make these devices somewhat sensitive to clock edge rates. The threshold level is typically 50% of $\rm V_{CC}$ for AC devices, and 30% of $\rm V_{CC}$ for ACT devices (1.5V at $\rm V_{CC}$ = 5V). Temperature has little effect on the clock threshold levels.

When clocking occurs, the internal gates and output circuits of the device dump current to ground, as previously mentioned. This condition results in a noise transient that is equal to the algebraic sum of internal and external ground-plane noise. When a number of loaded outputs change at the same time, it is possible for the chip ground reference level (and, therefore, the clock reference level) to rise by as much as 1V. If the clock input of a positive-edge-triggered

Two synchronized pulse generators are used to maintain input pulse-edge integrity for precise measurement fidelity. Generator 1 is used for driving only the measured buffer. Generator 2 is used for driving the other buffers.

device is at or near its threshold during a noise-transient period, multiple triggering can occur. To prevent this condition, the rise and fall slew rates of the clock inputs should be limited to the maximum ratings specified on the data sheet for the AC/ACT type. The AC/ACT 14 Hex Schmitt Trigger type is recommended for sharpening up slow transitions. Under the heading Power Consumption, the family rating for input rise and fall time is provided, and this topic is further expanded.

Maximum permissible input-clock frequency ratings on the data sheet for each clocked device require an input clock having a 50% duty cycle. At these rated frequencies, the outputs will swing rail to rail, assuming no DC load on the outputs. This feature provides a very conservative and highly reliable method of rating clock-input-frequency limits that, for the AC/ACT devices, equal or exceed the ratings for FAST types.

Low-Output Skew Flip-Flop Performance

AC/ACT flip-flop types such as the 74 dual D-type flip-flop are specially designed to have near equal delay from clock to Q and clock to \overline{Q} as illustrated in Figure 33. Dual slave sections are used to achieve this highly desirable performance. Actual delay skew between Q and \overline{Q} is typically 0.05ns and a Min/Max spread of 0.4ns at 85°C and a supply voltage (V_{CC}) of 5V. Figure 34 illustrates how this unique Harris flip-flop benefit can be used to drive a twisted pair. A termination R of about 300Ω is desirable to match the line and reduce reflections. The key element is near-zero skew at the Q and \overline{Q} output edges.

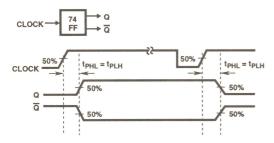


FIGURE 33. DELAY BALANCE OF DUAL D-TYPE FLIP-FLOP (AC/ACT74)

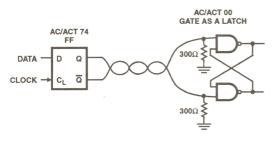


FIGURE 34. DUAL D-TYPE FLIP-FLOP (AC/ACT74) USED TO DRIVE A TWISTED PAIR

Metastability

Harris AC/ACT clocked devices are designed to minimize the probability of output states being at an undefined or unallowable condition because of violation of Clock/Data Setup time and Hold time specifications when used in asynchronous systems. Specifically, Setup and Hold times are kept small, typically Ons to 2ns. Also, internal flip-flop feedback paths are very fast with little delay. These design features serve to make metastability much less prevalent than for slower-speed CMOS or TTL Logic types.

Power Consumption

The power consumption of an AC/ACT device is composed of two components: one static, the other dynamic. The static component is the result of quiescent current caused principally by reverse junction leakage. The dynamic component results from the transient currents required to charge and discharge the capacitive loads on logic elements, that is, the transients resulting from the overlapping of active p and n transistors. Internal chip power consumption is determined by the device equivalent power dissipation capacitance, $C_{\rm PD}$; this parameter is defined below.

Power Calculations

Two equations are used to compute the total IC power consumption. Equation 2 is applicable to AC or ACT devices when the inputs are driven from ground to V_{CC} (rail to rail).

 $P = P_{DC} + P_{AC}$

$$P = I_{CC}V_{CC} + C_{PD}V_{CC}^2 f_i + \Sigma C_I V_{CC}^2 f_O$$

Whore

I_{CC} = Quiescent Current (from Data Sheet Ratings)

V_{CC} = Supply Voltage

f_i = Input Frequency

f_O = Output Frequency Per Output

C_{PD} = Device Equivalent Power Dissipation Capacitance; Used for Computing Internal Chip Power (from Data

C_L = Load Capacitance; Used for Computing Output Stage Power

Equation 3 is applicable only to an ACT device where specific input pins are driven at TTL levels defined as $V_{\rm I}=3.4V$ for a $V_{\rm CC}$ Max of 5.5V

$$\begin{split} P &= P_{DC} + P_{AC} \\ P &= I_{CC} V_{CC} + \Sigma \left(\Delta I_{CC} V_{CC} D + C_{PD} V_{CC}^2 f_i + C_L V_{CC}^2 f_0 \right) \end{split}$$

Where:

 ΔI_{CC} = Added direct current per input when $V_I = V_{CC}$ - 2.1V (TTL input high level) (from data sheet)

D = Duty cycle of clock (% of time high)

The temperature-dependent ratings for I_{CC} are given in Tables 9 and 10.

TABLE 9. TEMPERATURE-DEPENDENT RATING LIMITS

			+2	5°C	-40°C TO +85°C	-55°C TO +125°C
	V _I (V)	V _{CC} (V)	TYP (mA)	MAX (mA)	MAX (mA)	MAX (mA)
Δl _{CC} (Note 1)	V _{CC} - 2.1	4.5 to 5.5	0.2	2.4	2.8	3

NOTE

 Additional quiescent supply current per input pin, TTL inputs high, 1 unit load. ACT load table by type shown on each data sheet. Example: Type ACT191 input: clock unit load = 0.85 ΔI_{CC} = 0.85(2.4mA) = 2.04mA Max at +25°C.

TABLE 10. MAXIMUM QUIESCENT CURRENT AT V_{CC} = 5V FOR AC/ACT AND FAST TYPES

		FAST		
DEVICE				
COMPLEXITY	+25°C	+125°C		
SSVFF	4μΑ	40μΑ	80μΑ	15mA
MSI	8µА	80μΑ	160μΑ	100mA

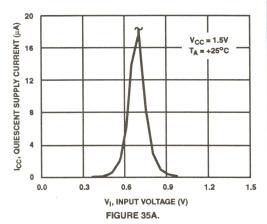
The dynamic power due to outputs is the sum of the AC power at each output. The user must independently determine the $\mathrm{C_L}$ and the average frequency of each output. The latter requires estimating the average frequency of data nodes in a logic system. For example, for AC/ACT counter types, each output is inherently operating at different frequencies.

The C_{PD}, or device equivalent-power-dissipation capacitance, is determined by two sources of internal device power consumption:

- Power consumed by charge and discharge of the internal device capacitance.
- 2. Power consumed through current switching transients.

Figure 35 illustrates the typical I_{CC} as a function of V_I for AC devices. Note in Figure 35C that when V_{IN} equals 0V to 0.5V or 4.5V to 5V, zero current flows. Thus, no ΔI_{CC} component is required for computing the power consumption of AC device types. The transient switching currents of an IC, however, consume power and are part of the C_{PD} value. The plots of I_{CC} and V_I of Figure 35 show peak I_{CC} of up to 12mA. For a few nanoseconds, however, up to 100mA could flow if the plotter resolution permitted. Note that the switching points (peak current points) in the AC devices occur at approximately 50% of V_{CC} . For the ACT devices (shown in Figure 36) the switching point is at approximately 30% of V_{CC} .

Figure 36 illustrates the typical I_{CC} as a function of V_I for ACT devices. Again, if the input voltage equals 0V to 0.5V or 4.5V to 5.5V, no ΔI_{CC} value exists. If V_I , however, is a TTL logic high level of 2.9V with a V_{CC} of 5V, then significant ΔI_{CC} does exist (0.2mA) and is indicated in Equation 3 as the ΔI_{CC} component.



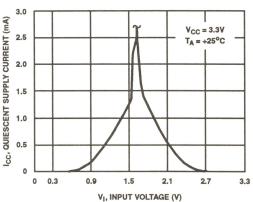


FIGURE 35B.

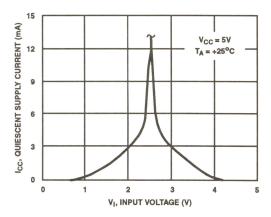


FIGURE 35C.

FIGURE 35. QUIESCENT SUPPLY CURRENT (I_{CC}) AS A FUNCTION OF INPUT VOLTAGE (V_I) FOR AC TYPES

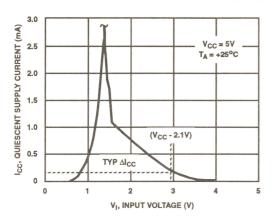


FIGURE 36. QUIESCENT SUPPLY CURRENT (I_{CC}) AS A FUNC-TION OF INPUT VOLTAGE (V_I) FOR ACT TYPES

In many TTL to CMOS ACT input interface applications only CMOS loads are driven and V_{OH} is 4V or more. As illustrated in Figure 36, ΔI_{CC} is 0 for TTL outputs only driving CMOS inputs. Only if a TTL output is fully loaded would the output V_{OH} be as low as 3V. Thus, ΔI_{CC} is usually negligible except in rare interfaces where full (15 fan out) TTL loading is present along with an ACT input.

Because the special input design of Harris ACT types reduces the value of ΔI_{CC} , the added power is small and is usually minimal compared to FAST power. If this special input circuitry were not used, the ΔI_{CC} values would be much higher.

Because appreciable current flows during device input switching, as shown in Figure 35 and Figure 36, it is important to maintain the fast input rise and fall times shown below.

INPUT RISE AND FALL SLEW RATE, dt/dv	MAX	UNITS	INPUTS
1.5V to 3V (AC Types)	50	ns/V	0 to V _{CC}
3.6V to 5.5V (AC Types)	20	ns/V	0 to V _{CC}
4.5V to 5.5V (ACT Types)	10	ns/V	0 to 3V

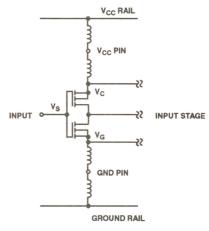
Because the typical output transition time is 3ns for AC/ACT types, a designer need only be concerned with exceeding the rise and fall slew rates shown above for interfacing or linear mode operation in applications such as RC oscillators, crystal oscillators, and the like.

When the Schmitt-Trigger type AC/ACT 14 is used either for shaping up slow signals or as an RC oscillator, power is increased by the prolonged through-current.

The adverse effect of power transitions is another reason to maintain input rise and fall slew rates under the recommended limits. Longer transitions may cause oscillations of logic circuits (and, hence, logic errors) or premature triggering, depending on the system V_{CC} and ground noise, which

are amplified when input signals hover near the switching voltages illustrated in Figure 35 and Figure 36. To reduce the effects of slower transitions, the use of Schmitt-Trigger types is recommended.

Simultaneous switching transients affect the maximum input $t_{\rm R}$, $t_{\rm F}$. Figure 37 illustrates a worst case but feasible condition for either a hex inverter type (04 or 05) or a hex inverting Schmitt-Trigger type (14). Using a printed circuit board designed for a ground-bounce measurement, five of six outputs are switched simultaneously causing the internal power or ground point bounce as discussed previously under the heading Simultaneous Switching Transients.



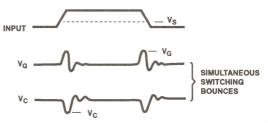


FIGURE 37. INPUT CIRCUIT AND SIMULTANEOUS SWITCHING BOUNCES THAT REDUCE NOISE IMMUNITY

Examination of the input stage and waveforms in Figure 37 shows clearly that typical noise immunity at the input is significantly reduced during the presence of the ground or V_{CC} bounce time as quantified below:

DC Noise Immunity Low
$$V_S$$
 - 0V = 2.5V (AC) = 1.5V (ACT) AC Noise Immunity Low V_S - V_G = 2.5V - 0.75V = 1.75V (ACT) DC Noise Immunity High V_{CC} - V_S = 2.5V (ACT) AC Noise Immunity High V_C - V_S = 1.5V (ACT) AC Noise Immunity High V_C - V_S = 1.5V (ACT) During V_{CC} Bounce = 2.5V (ACT)

Test results for the AC/ACT 04 and AC/ACT 14 types are illustrated in Figure 38. The results show that the real limiting values for input $t_{\rm R},\,t_{\rm F}$ slew rate times must take into account simultaneous switching effects. The Schmitt-Trigger type would ordinarily be considered to have nearly infinite slew rates for one-channel-only switching. For simultaneously switching five of six outputs, there is a probably finite limitation to slew rate times. However, tests for up to 150ms per volt for AC14 and 20ns per volt for ACT14 input slew rates (simultaneously on five inputs) did not affect the output.

$$V_{CC} = 5V, T_A = +25^{\circ}C$$

	MAXIMUM SLEW RATES					
TYPE	MEASURED (t _R)	PUBLISHED (t _F)				
AC04	> 20ns/V	20ns/V				
ACT04	>10ns/V	10ns/V				
AC14	290ms/V	150ms/V				
ACT14	40ns/V	20ns/v				

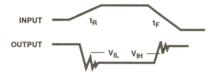


FIGURE 38. RESULTS OF TYPICAL INPUT t_R , t_F TESTS ON AC/ACTO4/14 TYPES. $V_{\rm CC}$ = 5V, T_A = +25°C. THE MAXIMUM VALUE OF t_R , t_F IS DEFINED FOR CONDITION THAT OUTPUT RINGING EXCEEDS $V_{\rm IL}$ OR GOES BELOW $V_{\rm IH}$ - FIVE OF SIX OUTPUTS ARE SWITCHING SIMULTANEOUSLY

Power Consumption of FAST and AC/ACT Types Compared

As the equations for operating power indicate, CMOS power is directly proportional to switching frequency. At standby, AC/ACT power is negligible compared to bipolar FAST power. In Table 11, one of the most widely used MSI counters (the 191 4-Bit Binary Counter) is used to illustrate that even at a continuous 10MHz switching rate, AC/ACT power is a fraction of the power of FAST types. By way of illustration, consider an application employing 25 such types. At an overall average switching rate of 10MHz, with FAST types the power is 7.7W; with AC/ACT types, the power is only 1.4W for AC types and 2.6W for ACT types.

TABLE 11. AVERAGE OPERATING POWER COMPARISON FOR FAST AND AC/ACT TYPE 191, A 4-BIT UP/DOWN BINARY COUNTER (V_{CC} = 5.5V; T_A = 70°C)

		SW			
FAMILY	NOTES	0MHz	1MHz	10MHz	UNITS
AC	1	0.44	5.5	55	mW
ACT	2	49.4	59.9	104	mW
FAST	3	204	224	306	mW

NOTES:

- 2. $P = P_{DC} + P_{AC}$. Where: $P_{DC} = 5.5 \times 80 \mu A$ and $P_{AC} = 133 p F(5.5)^2 f_1 + 50 p F(5.5)^2 + (1/2 + 1/4 + 1/8 + 1/16 + 1/16) f_0$ (See Equation 2)
- 3. $P = P_{DC} + P_{AC}$ Where: $P_{DC} = 5.5 \times 80 \mu A + 8 \times 2.8 mA \times 0.8 \times 1/2 \times 5.5$ (See Equation 3) and $P_{AC} = 133 pF(5.5)^2 f_1 + 50 pF(5.5)^2 + (1/2 + 1/4 + 1/8 + 1/16 + 1/16) f_0$ (See Equation 2)
- 4. P = 5.5 x 55mA (0Hz) P = 5.5 x 55mA x 1.1 (1MHz) P = 5.5 x 55mA x 1.5 (10MHz)

Special Harris AC/ACT Types

The Harris line of AC/ACT has some unique types that are tailored for specific high speed applications. Each is high-lighted below.

CD54/74 AC/ACT7623 - Octal-Bus Transceiver, Three-State (B-Side), Open-Drain (A-Side), Non-Inverting.

The only difference from the generic bipolar type 623 is that the 7623 has an open drain on the A-side; the 623 is three-state for both sides. The 7623 permits bus interfacing on the A-side without concern about bus contention. Also, the bus termination resistance is used to pull up the bus to a high state

CD54/74 AC/ACT7060 - 14-Stage Binary Counter with Oscillator.

The 7060 type is a 14-stage binary ripple counter having a built-in oscillator section (typically 200MHz) for either an RC design or an accurate crystal referenced design. A Master Reset input resets all binary stages to the all "0" state and also disables the oscillator when the Master Reset is high in the 7060 version.

References

JEDEC Standard No. 8. "Standard for Reduced Operating Voltages and Interface Levels for Integrated Circuits."

JEDEC Standard No. 20A, "Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High Speed CMOS Devices".

Family Ratings and Specifications ‡

Absolute Maximum Ratings (Note 1)

DC Supply Voltage, V_{CC} 0.5 to +6.0V DC Input Diode Current, I_{IK}	Power Dissipation po
For $V_1 < -0.5V$ or $V_1 > V_{CC} + 0.5V$	$T_A = -55^{\circ}C \text{ to } + 7$
DC Output Diode Current, I _{OK}	$T_A = +100^{\circ}C \text{ to } \cdot$
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	Package M
DC Output Source or Sink Current per Output Pin, Io	$T_A = -55^{\circ}C \text{ to } +7$
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$T_A = +70^{\circ}C \text{ to } +$
DC V _{CC} or Ground Current, I _{CC} or I _{GND} (Note 2) ±100mA	Operating Temperat
	Storage Temperature
	Lead Temperature (

ower Dissipation per Package, P_D
Package E
T_A = -55°C to +100°C......

T_A = +100°C to +125°C . . Derate Linearly at 8mW/°C to 300mW /2cakage M

 T_A = +70°C to +125°C Derate Linearly at 6mW/°C to 70mW verating Temperature Range, T_A 55°C to +125°C to +125°C rage Temperature, T_{STG} 65°C to +150°C

ead Temperature (During Soldering) At Distance 1/16in. ± 1/32in. (1.59mm ± 0.79mm)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges

4.5V to 5.5V (ACT Types) 10ns/V Max

DC Electrical Specifications - AC Series

						T _A , Al	MBIENT T	EMPERA	TURE (°C	C)	
		TEST C	ONDITIONS	V _{cc}	+25	5°C	-40°C TO) +85°C	-55°C T	O +125°C	
PARAMETERS	SYMBOL	V _I (V)	I _O (mA)	(V)	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
High-Level Input	V _{IH}			1.5	1.2	-	1.2	-	1.2	-	٧
Voltage				3	2.1	-	2.1	-	2.1	-	V
				5.5	3.85	-	3.85	-	3.85	-	V
Low-Level Input	V _{IL}			1.5	-	0.3	-	0.3	-	0.3	V
Voltage				3	-	0.9	-	0.9	-	0.9	٧
				5.5	-	1.65	-	1.65	-	1.65	V
High-Level Output	V _{OH}	V _{IH} or V _{IL}	-0.05	1.5	1.4	-	1.4	-	1.4		V
Voltage			-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	4.5	4.4	- "	4.4	-	4.4	-	٧
			-4	3	2.58	-	2.48	-	2.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	٧
			-75 (Notes 4, 5)	5.5	-	-	3.85	-	-	-	٧
			-50 (Notes 4, 5)	5.5	-	-	-	-	3.85	-	٧
Low-Level Output	V _{OL}	V _{IH} or V _{IL}	0.05	1.5	-	0.1	-	0.1	-	0.1	٧
Voltage			0.05	3		0.1	-	0.1	-	0.1	V
			0.05	4.5		0.1	-	0.1	-	0.1	V
			12	3		0.36	-	0.44	-	0.5	V
			24	4.5		0.36	-	0.44	-	0.5	V
			75 (Notes 4, 5)	5.5		-	-	1.65	-	• /	٧
			50 (Notes 4, 5)	5.5	-	-	-	-		1.65	٧

For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX.
 See Section 8, "How to use AnswerFAX", in this selection guide.
 3-23

Family Ratings and Specifications‡

DC Electrical Specifications - AC Series (Continued)

				T _A , AMBIENT TEMPERATURE (°C)						C)	
		TEST C	TEST CONDITIONS		+25	5°C	-40°C TO	+85°C	-55°C T	O +125°C	
PARAMETERS	SYMBOL	V _I (V)	I _O (mA)	V _{CC} (V)	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
Input Leakage Current	I _I	V _{CC} or GND		5.5	-	±0.1	-	±1	-	±1	μА
Three-State Leak- age Current (Note 6)	I _{OZ}	V_{IH} or V_{IL} , $V_{O} = V_{CC}$ or GND		5.5	-	±0.5		±5	-	±10	μА
Quiescent Supply Current, MSI (Note 7)	I _{CC}	V _{CC} or GND	0	5.5	-	8 ,	-	80	-	160	μА

DC Electrical Specifications - ACT Series

						T _A , Al	MBIENT T	EMPERA	TURE (°	C)	
		TEST C	ONDITIONS	V _{cc}	+25	5°C	-40°C TO	O +85°C	-55°C T	O +125°C	
PARAMETERS	SYMBOL	V _I (V)	I _O (mA)	(V)	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
High-Level Input Voltage	V _{IH}			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	V _{IL}			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output	V _{OH}	V _{IH} or V _{IL}	-0.05	4.5	4.4	-	4.4	,-	4.4	-	V
Voltage			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Notes 4, 5)	5.5	-	-	3.85	-	-	-	V
	-		-50 (Notes 4, 5)	5.5	-	-	-	-	3.85	-	V
Low-Level Output	V _{OL}	V _{IH} or V _{IL}	0.05	4.5	-	0.1	-	0.1	-	0.1	V
Voltage			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Notes 4, 5)	5.5	-	-	-	1.65	-	-	V
			50 (Notes 4, 5)	5.5	-	-	-	-	-	1.65	٧
Input Leakage Current	I _I	V _{CC} or GND		5.5	-	±0.1	-	±1	-	±1	μА
Three-State Leak- age Current (Note 6)	l _{oz}	V_{IH} or V_{IL} , V_{O} = V_{CC} or GND		5.5		±0.5	-	±5	-	±10	μА
Quiescent Supply Current, MSI (Note 7)	I _{CC}	V _{CC} or GND	0	5.5	-	8	-	80	-	160	μА
Additional Supply Current per Input Pin, TTL Inputs High, 1 Unit Load	Δl _{CC}	V _{CC} - 2.1		4.5 to 5.5	-	2.4	-	2.8	-	3	mA

NOTES:

- Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
- 2. For up to 4 outputs per device; add ±25mA for each additional output.
- 3. Unless otherwise specified, all voltages are referenced to ground.
- 4. Test one output at a time for a 1s maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
- 5. Test verifies a minimum 50Ω transmission-line-drive capability at +85°C, 75Ω at +125°C.
- 6. Three-State devices only (off-state leakage current for open-drain types).
- 7. SSI/FF limits are 4µA at +25°C, 40µA at 0°C to +70°C, -40°C to +85°C, 80µA at -55°C to +125°C.

For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX.
 See Section 8, "How to use AnswerFAX", in this selection guide.
 3-24

Operating and Handling Considerations

Handling

All inputs and outputs of Harris CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in Application Note, AN6525, AnswerFAX document number 96525, "Guide to Better Handling and Operation of CMOS Integrated Circuits." See Section 8, "How to Use AnswerFAX" of this selection guide.

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{CC} - GND to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{CC} nor less than GND. Input currents must not exceed 20mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or GND, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{CC} or GND may damage CMOS devices by exceeding the maximum device dissipation.

Substrate Connection

When devices in chip form are used in hybrid applications, the substrate is connected to GND (as with all P-substrate devices).

Enhanced Product

Features

- Enhanced Advanced CMOS Logic is Burned-In and has a tighter AQL than standard product.
- · Burn-In Time (Note 1) 160 Hours
- · Bias Voltage 6V
- Identification is by an added suffix X to the standard brand.
- · Examples for the 00 type in the plastic DIP package
 - CD74AC00EX or CD74ACT00EX

Applications

The need to achieve the enhanced reliability resulting from burn-in screening must be determined by careful analysis of system design and application.

How many IC's are incorporated into the total system?

How many devices on each board?

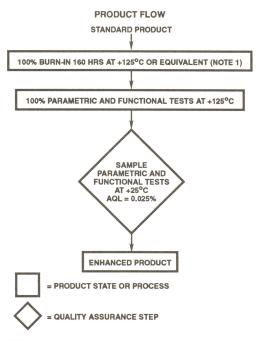
Is the proper device being used for the application? What are the reliability goals?

What failure rates are being experienced without screening?

Cost-effectiveness of using enhanced CMOS can be determined by mutual analysis of the economic trade-offs made possible by the following features of the program:

- Available in Plastic Package (Dual-In-Line)
- · Offered on the Industry's Broadest Line of Circuit Functions
- 0.025% AQL Cumulative; AQL on Standard Product is 0.065 % a Cumulative
- Reduction in PC Board Reworking Through Fewer Line Rejects
- Lower Warranty Requirements Through the Elimination of Infant Mortality Failures

- Reduced Incoming Inspection Cost by Reduction or Complete Elimination of Test Procedures
- Reduction of System Failures and Related Service Expenses and Customer Complaints



NOTE:

 Or equivalent means equivalent time-temperature/voltage resulting in the same activation energy.



CMOS LOGIC ICs

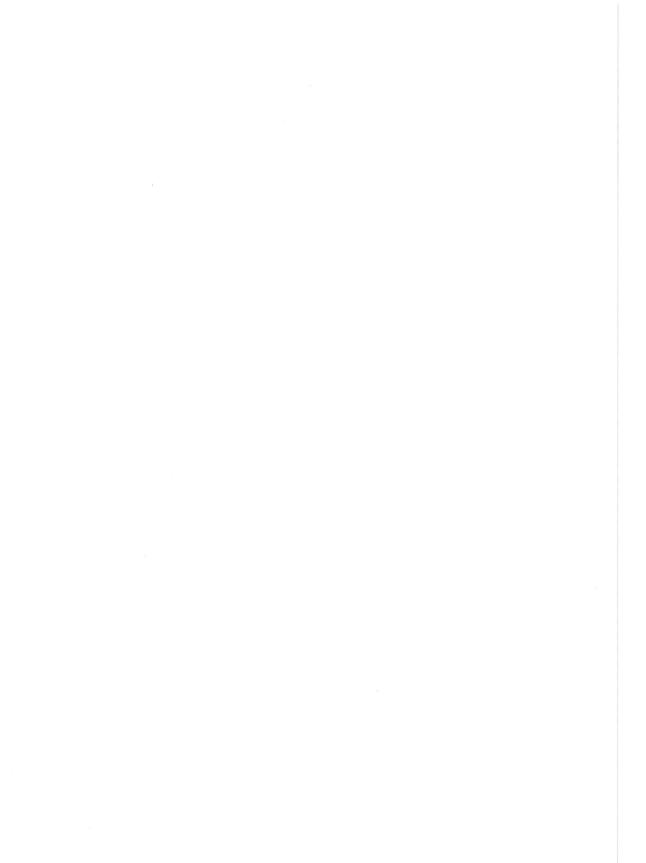
4

PRODUCT SELECTION GUIDE

BICMOS INTERFACE LOGIC - FCT SERIES

	PAGE
CROSS REFERENCE GUIDES	4-3
TECHNICAL OVERVIEW	4-5
Features	4-5
Applications	4-6
FCT IC Process Technology	4-6
Input Protection.	4-7
Input Structure	4-7
Output Structure	4-8
Ground Bounce and Simultaneous Switching Transients	4-8
Latch-Up Sensitivity	4-10
DC Electrical Specifications	4-10
Dynamic Characteristics.	4-12
Power Consumption	4-17
System Design Considerations.	4-18
References	4-20
FAMILY RATINGS AND SPECIFICATIONS‡	4-21
OPERATING AND HANDLING CONSIDERATIONS	4-22

For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX. See Section 8, "How to use AnswerFAX", in this selection guide.
4-1



Cross Reference Guides

TABLE 1A. CROSS OF AN IDT TYPE TO A RECOMMENDED HARRIS REPLACEMENT TYPE

IDT TYPE	HARRIS REPLACEMENT
Р	Е
so	М
xxx	XXX
XXXA	XXXAT
XXXT	XXX
XXXAT	XXXAT
8XXA	8XXA

Type Numbers that cross over with one or more of the six options shown (XXX) in the above table.

240	373	543	652	841A	863A
241	374	573	821A	842A	
244	533	574	822A	843A	
245	540	646	823A	844A	
273	541	651	824A	861A	

Special Type Number Crossovers Applicable to IDT Type Cross Reference.

IDT FUNCTION	HARRIS FUNCTION
IDT29FCT52A	CD74FCT2952A
IDT29FCT52AT	CD74FCT2952A

TABLE 1B. CROSS OF IDT/FCT GENERAL PURPOSE LOGIC TYPES TO HARRIS ACT GENERAL PURPOSE LOGIC TYPE EQUIVALENTS

Harris CD74ACTXXXE/M logic types are described and specified in Section 3 of this selection guide.

Characteristics common to IDT/FCT logic types listed here are the same as Harris ACT logic types with the same part numbers.

- · TTL Switch Level at Inputs
- Logic Function and Pinout
- Output Swing to 3.3V or More; i.e., TTL Output Level or Rail-To-Rail Output Swing

Characteristics that May Differ:

- · Switching Speed See Specifications
- SINK/SOURCE Current See Specifications
- Input or output clamp diodes to V_{CC}. All Harris ACT types have I/O clamp diodes to V_{CC}. IDT/FCT logic types vary from type to type in I/O clamp diodes to V_{CC}. See IDT specifications.

IDT/FCT LOGIC TYPE	HARRIS ACT EQUIVALENT LOGIC TYPES
IDT74FCTXXX	CD74ACTXXX
IDT74FCTXXX	CD74ACTXXX
IDT74FCTXXXT	CD74ACTXXX
IDT74FCTXXXT	CD74ACTXXX
IDT74FCTXXXA	CD74ACTXXX
IDT74FCTXXXA	CD74ACTXXX
IDT74FCTXXXAT	CD74ACTXXX
IDT74FCTXXXAT	CD74ACTXXX

Type Numbers that cross over with one or more of the options shown (XXX) in Table 1B.

151	138	191
157	139	193
251	161	299
257	163	

TABLE 2. CROSS OF EQUIVALENT BIPOLAR FAST TTL TYPE
TO HARRIS RECOMMENDED REPLACEMENT

BIPOLAR FAST TYPE	HARRIS REPLACEMENT		
74FXXXP	CD74FCTXXXE		
74FXXXS	CD74FCTXXXM		

Type Numbers that cross over (XXX) in the above table.

240	373	543	623	821A (Note 1)
241	374	544	646	823A (Note 1)
244	533	564	651	841A (Note 1)
245	540	573	652	843A (Note 1)
273	541	574		

NOTE:

^{1.} FCT equivalent types have a suffix A designation; the F types do not.

TABLE 3. CROSS OF EQUIVALENT BIPOLAR AS/TTL TYPES TO HARRIS RECOMMENDED REPLACEMENT TYPES

BIPOLAR AS/TTL TYPE	HARRIS REPLACEMENT	
SN74ASXXXN	CD74FCTXXXE	
SN74ASXXXDW	CD74FCTXXXM	

Type Numbers that cross over (XXX) in the above table.

240	533	652	842A (Note 1)
241	573	821A (Note 1)	843A (Note 1)
244	574	822A (Note 1)	844A (Note 1)
245	623	823A (Note 1)	
373	646	824A (Note 1)	
374	651	841A (Note 1)	

NOTE:

1. FCT equivalent types have a suffix A designation; the AS types do not.

TABLE 4. CROSS OF EQUIVALENT BIPOLAR ALS/TTL TYPE
TO HARRIS RECOMMENDED REPLACEMENT

BIPOLAR ALS/TTL TYPE	HARRIS REPLACEMENT
SN74ALSXXXN	CD74FCTXXXE
SN74ALSXXXN-1	CD74FCTXXXE
SN74ALSXXXDW	CD74FCTXXXM
SN74ALSXXXDW-1	CD74FCTXXXM

Type Numbers that cross over (XXX) in the above table.

ALS	FCT	ALS	FCT	ALS	FCT
240A	240	540	540	652	652
241A	241	541	541	653	653
244A	244	564	564	654	654
245A	245	573	573	841	841A
273	273	574	574	842	842A
373	373	623A	623	843	843A
374	374	646	646	844	844A
533	533	651	651		

TABLE 5. CROSS OF EQUIVALENT TI BICMOS BCT TYPE TO HARRIS RECOMMENDED REPLACEMENT

TI BCT TYPE	FCT TYPE	
SN74BCTXXXN	CD74FCTXXXE	
SN74BCTXXXDW	CD74FCTXXXM	

Type Numbers that cross over (XXX) in above table.

240	374	564	651
241	533	573	652
244	540	574	
245	541	623	
373	543	646	

Additional BCT/FCT Crossover Types:

ВСТ	FCT	вст	FCT	вст	FCT
29821	821A	29841	841A	29861	861A
29822	822A	29842	842A	29863	863A
29823	823A	29843	843A		
29824	824A	29844	844A		

TABLE 6. CROSS OF EQUIVALENT AMD "29" SERIES BIPOLAR OR CMOS LOGIC TYPE TO HARRIS RECOMMENDED REPLACEMENT TYPE

CATEGORY	AMD TYPE	HARRIS FCT TYPE	
800 Series	AM29XXX	CD74FCTXXXA	
	AM29XXXC	CD74FCTXXXA	
Specific Nos.	AM2952	CD74FCT2952A	

The suffix A Harris FCT replacement types are generally faster speed than equivalent AMD "29" series types.

Type Numbers that cross over (XXX) in above table.

821	823	841	843	861
822	824	842	844	863

Features

Harris FCT is a broad family of 8-bit, 9-bit and 10-bit computer-bus interface logic ICs. Harris FCT BiCMOS Bus-Interface ICs are designed to satisfy four major requirements of modern bus-oriented computer systems, namely:

- · High Speed/Low Propagation Delay
- High Drive, to Meet Specified Bus-Interface Requirements for Clock and Data Lines
- Low Power Consumption (CMOS-Like)
- · Minimization of Switching Noise

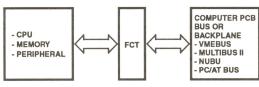


FIGURE 1. FCT AS BUS-INTERFACE ICs

NOTE: Harris offers FCT products in two speed grades: base speed (equal to FAST speeds) and higher speed (on average, 30% faster). The base speed version of each type is designated as either FCT or FCTXXXA, and the higher speed version, FCTXXXAT. The "T" was added to the suffix in order to highlight the fact that Harris FCT devices have a TTL-like output swing. Throughout this technical overview, FCT, FCTXXXA, FCTXXXAT are referred to collectively as FCT.

Clearly there is no other bus-interface logic family that meets all four of these system requirements as well as Harris FCT does. Other bus-interface families such as AS, F (FAST), BCT, and BC have higher power consumption (See Figure 2) and lower speed (See Figure 3). Also, the Harris BiCMOS technology, being CMOS based with only modest additional complexity for the bipolar circuitry, has lower manufacturing costs than other more complex BiCMOS processes.

For non-8-bit, non-9-bit and non-10-bit bus-interface functions, the logic family of choice for low-power, advanced high speed performance is the Harris AC/ACT family.

The many excellent features of the new Harris FCT BiCMOS bus-interface logic family are detailed in Table 1.

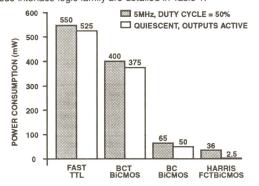


FIGURE 2. POWER CONSUMPTION COMPARISON, BUS-INTERFACE LOGIC FAMILIES

TABLE 1. FEATURES OF THE HARRIS FCT FAMILY

FEATURES	
High Speed, Typical Delay = 3.5ns	
FCTXXXAT is faster than FAST	
Low Power	Typical Power/Function
Quiescent	0mW
5MHz	5.6mW
10MHz	11.2mW
Output Sink Current	
Buffers	
FF/Latches	
Limited Output Voltage Swing (for reduce 3.5V Typical	ced noise generation)
No Diode Clamps from Inputs or Output	ts to V _{CC}
Minimized Switching Noise Design, Lay Low Ground Bounce - Typically 1.2\	
Reduced EMI Due to Slowed Output	t Edges
Good Input Dynamic Noise Immunity and input hysteresis)	(via isolated ground system
ESD: ±2kV (HBM)	
Not Latch-Up to Above ±300mA	
Variety of Bus-Interface Functions	
Buffers	Octal
	10-Bit
Flip-Flops/Registers	Octal
	9-Bit
	10-Bit
	Special Registers
Transceivers	Octal
	9-Bit
	10-Bit
Latches	Octal
	9-Bit
	10-Bit

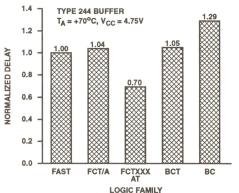


FIGURE 3. NORMALIZED PROPAGATION DELAY, AVERAGE OF t_{PLH}, t_{PHL}, t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH} MAXIMUMS (ADJUSTED FOR TEMPERATURE AND VOLTAGE WHERE NECESSARY)

Applications

Meeting Bus Standards

As illustrated in Table 2, Harris FCT bus-interface ICs match up ideally to the popular VMEbus, Multibus II, and other open or proprietary bus standards that require similar high speed performance and high sink-current capability.

TABLE 2. 32-BIT COMPUTER BUS STANDARDS

BUS	IEEE STD. NO.	DRIVER TECHNOLOGY
VMEbus	1014	TTL/FCT
NuBus	1196	TTL/FCT
Multibus II	1296	TTL/FCT
IBM Micro Channel Architecture (MCA)	None	TTL/FCT
Extended Industry Standard Architecture (EISA)	None	TTL/FCT
Sun Microsystems Sbus	None	CMOS/FCT

FCT vs AC/ACT Use

The new Harris FCT bus-interface products complement the existing popular Harris AC/ACT logic family. The fundamental difference between these two families is that FCT is capable of sinking the 48mA or 64mA required for back-plane interface, while the AC/ACT family parts provide a balanced ±24mA output drive current capability in all logic and businterface family members. Table 3 describes the application of FCT vs AC/ACT.

FCT IC Process Technology

Harris FCT devices are fabricated in a 1.5μm BiCMOS process (See Figure 4). The basis of this process is a silicongate CMOS, double-level-metal, N-well configuration. To this, the necessary steps are added to create an additional physical layer called P ISO. The P ISO layer is used to construct uncommitted diodes and uncommitted bipolar NPN transistors. (Intrinsic diodes and bipolar transistors exist in processes that lack this additional layer, i.e. pure CMOS processes, but these devices are not uncommitted).

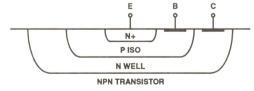


FIGURE 5. SIMPLIFIED DRAWING OF BIPOLAR NPN TRANSISTOR

A heavily doped P substrate is topped with a thin epitaxial layer of lightly doped P material. The heavy doping of the substrate and small geometries within the epitaxial layer minimize the resistances encountered in these regions, thereby virtually eliminating the occurrence of latch-up. Injected currents flow through the low impedance substrate to ground without triggering any parasitic SCRs (See Latch-Up Sensitivity in this section).

The self-aligning nature of the silicon-gate process serves to reduce parasitic capacitance associated with the CMOS transistors, thereby increasing performance of the circuitry. Two levels of metallization provide for more efficient routing of interconnect, power and ground lines.

TABLE 3. FCT vs AC/ACT APPLICATION

APPLICATION	FCT	AC/ACT
1. Drive Worst Case VME, Multibus II, or other backplane specified around higher power FAST TTL bus drivers. Requires 64mA sink current for clocks and strobes. 330Ω 470Ω BACK PLANE 5V 330Ω 470Ω 470Ω	Yes	No
2. Drive 50Ω PCB trace, coax, twisted pair, flat cable, etc. Maintain incident edge switching at both ends or any tap. (Source current of FCT is not sufficient.)	No	Yes
Highest speed, lowest power, most noise immune logic system or bus interface system without line termi- nations	No	Yes (AC)
Driving memory input or CMOS Logic/ASIC inputs that require a balanced rail-to-rail logic swing	No	Yes
Bus Interfaces that need 24mA or less sink current	Yes	Yes
Interfaces between equipment with separate power supplies	Yes (No I/O Clamp Diodes)	No
Complete logic family including SSI (Gates) and MSI logic functions	No	Yes

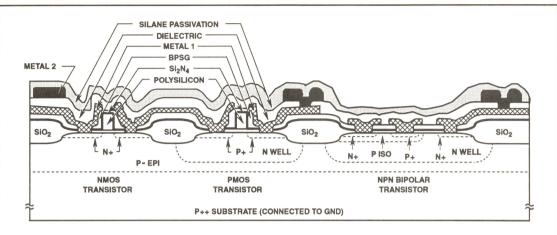


FIGURE 4. HARRIS FCT BICMOS 1.5μm PROCESS CROSS SECTION

Input Protection

FCT device inputs are protected by the network shown in Figure 6. This network protects the device against electrostatic discharge (up to at least 2kV for the human body model), which occurs in the normal handling of such components, as well as transients associated with normal operation in a system environment.

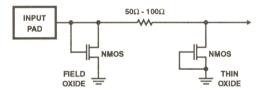


FIGURE 6. FCT INPUT PROTECTION NETWORK

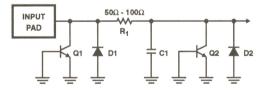


FIGURE 7. PARASITIC ELEMENTS IN THE CIRCUIT OF FIGURE 6

The operative elements in the protection mechanism are actually parasitic devices that exist in the network. These are shown in Figure 7. Whenever two N-type regions are formed within a P-type material to create an NMOS transistor, a parasitic NPN bipolar transistor results. The P-material, which is tied to ground, acts as the base. Q1 in Figure 7 is the NPN device associated with the field oxide NMOS transistor in Figure 6, and Q2 results from the construction of the thin oxide NMOS device. Diode D1 and Diode D2 are actually the base-collector junctions of transistor Q1 and transistor Q2, respectively, but are drawn separately for illustration. Primary protection is provided by Q1, which will go into breakdown for positive input voltages greater than

about 15V. (The gate oxide of the input inverter that follows the protection can withstand up to about 25V to 30V). For negative input voltages, diode D1 simply conducts in the forward region. Secondary protection is provided by the remaining components, R1, C1, Q2 and D2. The combination of R1 and C1 will attenuate high speed transients, and Q2/D2 will behave in a similar manner to Q1/D1. The field oxide NMOS device itself would turn on if the input reached a level of about 18V.

Input Structure

The circuit diagram for the input structure of Harris FCT devices is shown in Figure 8.

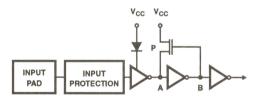


FIGURE 8. FCT INPUT STRUCTURE

The details of the input protection circuit are discussed in the preceding section. Following the input protection network is an inverter stage designed for TTL level inputs. The switch-point of the inverter is lowered from the typical $V_{\rm CC}/2$ value for CMOS level inputs to a value near the middle of the range between the TTL $V_{\rm IH}$ and $V_{\rm IL}$ limits. A simple method for lowering the switchpoint of an inverter is to increase the width of the N-transistor. However, using this method alone requires a considerable increase in the size of the N-transistor. The total increase in chip area becomes significant when this is done for all inputs. So, instead of using all of this chip area, Harris has added a diode to the $V_{\rm CC}$ line of the inverter. The diode itself lowers the switchpoint by one diode drop, thereby allowing for a much smaller increase in the width of the N-transistor.

The diode also lowers the output high level of the input inverter by one diode drop. So, in order to reduce flow-through current in the next stage, a P-transistor pull-up is used. This device turns on after node A switches high and node B switches low, and then pulls node A all the way up to the rail.

An additional benefit of the P-transistor is that it requires a slightly higher input voltage to switch node A back low again. This input hysteresis provides added immunity against ground bounce and other similar transients on the inputs.

Output Structure

The circuit diagram for the output stage used in Harris FCT devices is shown in Figure 9.

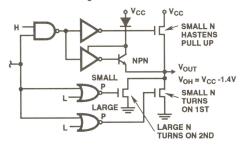


FIGURE 9. HARRIS FCT OUTPUT STAGE

Output Source Structure

The pull-up structure of FCT outputs is designed to eliminate the intrinsic protection diode from the output to V_{CC} , and to limit the output high voltage (V_{OH}) to 2 diode drops below V_{CC} .

The intrinsic protection diode to V_{CC} is removed by eliminating the P-transistor that would appear in a pure CMOS output structure. Instead of a P-channel pull-up, a bipolar NPN transistor in an emitter follower configuration is used. A small N-transistor is also used in parallel with the NPN, but the former drops out as the output voltage rises (i.e. as its gate to source voltage decreases). The benefits of eliminating the intrinsic diode to V_{CC} are ease of application in bus systems utilizing multiple power supplies, and in battery backed-up systems or other systems that are partially powered down. To provide protection for the outputs, a protection network is used that is similar to the input protection network, but without the series resistor.

The supply level for the collector of the NPN transistor and the inverter preceding the transistor is one diode drop below the $V_{\rm CC}$ level for the rest of the chip. The high level output of the inverter (i.e. the base of the NPN) is thus limited to one diode drop below $V_{\rm CC}$. In turn, the high level voltage at the output pin, from the emitter of the NPN transistor, follows the base voltage minus the diode drop across the base emitter junction. The advantages of a reduced output swing are reduced ground bounce and reduced EMI generation. Both of these result from the slower edge rate produced by decreasing the change in voltage for a given change in time. More information on ground bounce and EMI is available in other sections of this overview and in the references listed at the end of the overview.

Output Sink Structure

The pull-down structure of FCT outputs (also shown in Figure 9) is designed to sink 48mA/64mA under static conditions (more on a dynamic basis), and to spread out over time the transient current associated with switching the outputs.

The distribution of transient current is achieved through the use of two, differently sized N-transistors in parallel. The logic gates driving the N-transistors are designed such that the smaller N turns on first. This smaller N-transistor discharges the capacitive load at a slower rate than the larger device, resulting in lower ground bounce. The larger N-transistor, which is needed to provide the bulk of the static drive capability, turns on after the transient current (and $V_{\rm OLP}$) have already peaked (See Figure 10). For more information on ground bounce/ $V_{\rm OLP}$ see the following section entitled Ground Bounce and Simultaneous Switching Transients.

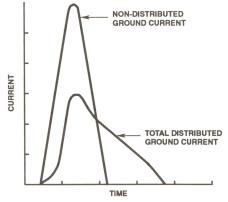


FIGURE 10A. NON-DISTRIBUTED vs TOTAL DISTRIBUTED

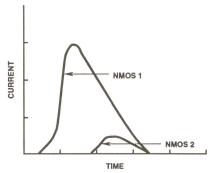


FIGURE 10B. COMPONENTS OF TOTAL DISTRIBUTED CURRENT
FIGURE 10. TRANSIENT SINK CURRENT

Ground Bounce and Simultaneous Switching Transients

Ground bounce and $V_{\rm CC}$ bounce are caused by the transient currents associated with switching capacitive loads. These transient currents cause voltage spikes across intrinsic inductances in the output source and sink paths of digital logic devices (See Figure 11).

Figure 12 shows the case of an FCT output switching from high to low. Transient current i flows through the total intrinsic inductance to system ground, causing a peak voltage differential (V_{LMAX}) between the on-chip ground and the system ground.

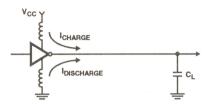


FIGURE 11. OUTPUT TRANSIENTS DUE TO LOAD CAPACITANCE

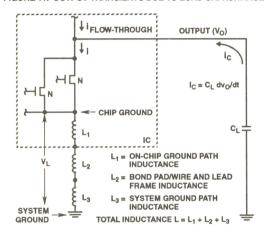


FIGURE 12. INDUCTANCES AND TRANSIENT CURRENTS RELATED TO GROUND BOUNCE

 V_{LMAX} is seen as the positive peak value of the voltage waveform appearing across the inductance. This waveform (V_L) is shown in Figure 13 and is described by the following equation:

$$V_{L} = L \frac{di}{dt}$$
 (EQ. 1)

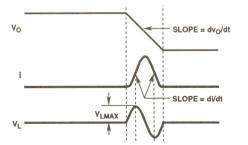


FIGURE 13. WAVEFORMS FOR CIRCUIT OF FIGURE 12

This internal ground bounce is coupled through the chip to the other outputs of the device, where the peak is measured as V_{OLP} . The magnitude of V_{OLP} for a given output depends on the magnitude of V_{LMAX} and the characteristics of the signal path for that particular output.

Since all of the device outputs have a common ground, the transient currents, and hence the likelihood of higher internal ground bounce, will increase with the number of outputs switching simultaneously. Also, there is mutual coupling among output signal paths which causes varying levels of V_{OLP} for a given output, depending on the particular combination of outputs that are switching simultaneously.

Worst case V_{OLP} for ICs with end pin V_{CC} and GND is measured at the output located farthest from the GND pin with all other outputs switching simultaneously from high to low. See Application Note AN9001, "Measurement of Ground and V_{CC} bounce in Advanced High Speed (AC/ACT/FCT) CMOS Logic ICs". See Section 8, "How to Use AnswerFAX" of this selection guide.

Reducing Ground Bounce

Taking another look at Equation 1 and noting that (i) itself is a function of dv_O/dt , it is seen that either a reduction in total inductance (L) or a reduction in the rate of change of the output edge (dv_O/dt) will result in decreased internal ground bounce. Harris has taken steps in both of these directions to reduce ground/V $_{\rm CC}$ bounce and simultaneous switching transients in FCT devices.

- Layout techniques are used to reduce on-chip inductance in the V_{CC} and ground paths, especially for the segments that are common to all outputs. (See L1 in Figure 12).
- Multiple bond-pads and bond-wires are used for V_{CC} and GND to reduce the inductance, in those paths, between the chip and the lead. (See L2 in Figure 12).
- Lead frames are modified to create a ground plane. This also reduces L2.
- By switching from 0V to 3.5V, Harris FCT outputs provide a reduction in dv_O/dt over parts that switch from 0V to 5V in the same amount of time.
- Additionally, for high to low output transitions, the distributed pull-down structure lowers di/dt by reducing the peak amplitude and increasing the duration of the transient current waveform.

(For item 4 and item 5 above, see the output structure description under this heading).

 V_{OLP} is further reduced in Harris FCT through the use of layout techniques that minimize the mutual coupling among outputs, and also between inputs and outputs.

Input Hysteresis

In addition to reducing ground bounce/V_{OLP}, Harris has increased the immunity of FCT to such transients, as well as any other ground noise, by adding hysteresis to the inputs. (See the input structure discussion earlier in this overview).

Latch-Up Sensitivity

Latch-up is an undesired state which occurs when a parasitic SCR, formed in ICs containing CMOS circuitry, is triggered. This parasitic SCR structure is shown in Figure 14. Triggering is caused by overvoltages or undervoltages (on input, output, or supply pins) which cause current to be injected into the substrate (i.e. to flow through substrate diodes). Once the device is triggered, a low impedance path is formed between $V_{\rm CC}$ and GND, thus allowing potentially destructive current ($I_{\rm C}$) to flow through the chip.

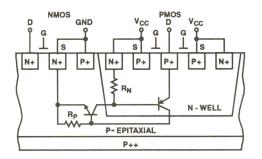


FIGURE 14A. CROSS SECTION OF CMOS STRUCTURE SHOW-ING SCR LATCH-UP PARASITIC TRANSISTOR

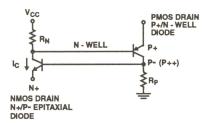


FIGURE 14B. SIMPLIFIED DIAGRAM
FIGURE 14.

The Harris FCT process employs a thin epitaxial layer of lightly doped P material. This allows for heavier doping of the P substrate, which lowers the resistance of the substrate. The resistance of the EPI layer is limited by its small thickness and through liberal use of contacts to GND. Similarly, the N-well resistance is limited by its dimensions and through the use of contacts to $V_{\rm CC}$. Lowering the resistance of these regions increases the amount of current required to produce the biasing voltages needed to turn on the bipolar transistors, thereby significantly reducing the probability of triggering a parasitic SCR.

The use of the EPI layer, contacts, and other design and layout techniques result in resistance to latch-up for transient currents up to over 400mA, typical, at any input or output. The absolute maximum DC rating, as specified in the JEDEC Standard No. 18, is -20mA at the inputs and -50mA at the outputs.

DC Electrical Specifications

All DC and AC specifications of Harris FCT Bus-Interface ICs meet the industry standard JEDEC Standard No. 18 specifications.

Absolute Maximum Ratings

Note the conservative +6V absolute maximum DC supply voltage which, literally, means that Harris reliability data is based on long term operation at 6V and +125°C. For short term overvoltage and conducted transients, the supply voltage can increase to 10V or more. For the maximum rated DC input, output, V $_{\rm CC}$, and ground currents shown, Harris design rules for internal chip metallization cross sections are such that there is no long term degradation of the Si-Al interconnect traces. Peak switching transient currents for V $_{\rm CC}$, ground, and output traces may be higher (up to 1A) and are easily handled by the generous cross sectional area of the interconnect.

For free air power dissipation the thermal resistance of the plastic DIPs is 125°C/W, and for SOPs is 167°C/W.

Recommended Operating Conditions

All plastic packaged 74 series devices are reliably operated over the full temperature range of -55°C to +125°C. The recommended input slew rate of 10ns/V translates to the following maximum rise and fall times:

 $V_{IN} = 3V$; t_{R} , $t_{F} \le 24$ ns, 10% to 90%

 $V_{IN} = 5V$; t_{R} , $t_{F} \le 40$ ns, 10% to 90%

Please make note of the fact that switching speeds are specified and tested for input rise and fall times of 3ns.

For practical application purposes, the switching speeds and power dissipation prediction equations (shown later in this overview) are useful for up to 10ns input rise and fall times. There exists a range of capacitive loading (up through 150pF) for which FCT outputs will be within this range.

DC Electrical Specifications

The Harris FCT family DC ratings are shown in the DC Electrical Specifications table. Refer to Table 4 for the bytype output sink current (I_{OL}) and output source current (I_{OH}). Note that the critical I_{CC} quiescent current is 80 μ A at +70°C. The JEDEC limit, and competition's specification, is 1.5mA. Clearly, for battery power or battery back-up the Harris FCT is the preferred product.

Input Current vs Input Voltage

Figure 15 is the typical $I_{\rm IN}$ vs $V_{\rm IN}$ characteristic at $T_{\rm A} = +25^{\circ}{\rm C}$ for FCT devices. From $V_{\rm IN} = 0{\rm V}$ to 10V the only current flowing is leakage current (typically 100nA). At about -0.8V the input diode to ground starts to conduct. This diode clamps the input voltage at approximately -1V. Under this condition input current should be limited to -20mA DC; 1A for peak transients of a few ns. Switching Current vs Input Voltage, Figure 16, shows the typical DC switching characteristics for an FCT input. Current (between $V_{\rm CC}$ and ground) begins to flow at approximately 0.7V and peaks at

about 1.4V. At the maximum current point the N and P transistors are both on and present the least resistance between V_{CC} and ground. Note that for a typical TTL V_{IL} of 0.25V to 0.4V, I_{CC} is below 1 μ A.

Sink Current Capability (IOL vs VOL)

Figure 17 shows the typical output sink capability of an FCT 240 under various conditions from worst case, at $V_{\rm CC}=4.5V$ and $T_{\rm A}=+125^{\circ}C$, to best case, at $V_{\rm CC}=5.5V$ and $T_{\rm A}=-55^{\circ}C$. At $V_{\rm OL}=0.55V$, the output voltage at which 64mA is specified (at 5V, +25°C and 4.75V, +70°C) the curves indicate typical values of 120mA and 90mA, respectively. For $V_{\rm CC}=4.5V$ and +125°C, and $V_{\rm OL}=0.55V$, the curve shows a typical value of 80mA which far exceeds the 48mA specified in the DC Electrical Specifications chart.

Source Current Capability (IOH vs VOH)

Figure 18 shows the typical output source capability under the same conditions as in Figure 17. In these curves, at V_{OH} = 2.4V the typical currents at +25°C and +70°C are -69mA and -49mA, respectively; the minimum limit is -15mA. At +125°C and V_{OH} = 2.4V the curve shows -35mA; the minimum specified value is -12mA.

At the colder temperatures of 0°C and -55°C the current drive, both sink and source, is substantially higher.

The X-intercepts of Figure 18 show the FCT output voltage for CMOS input loads (defined as $I_{IN} = 1\mu A$, typically I_{IN} is a few nA). Table 5 summarizes V_{OH} for strictly CMOS loads. The data in this table is useful in FCT-to-CMOS (HC/HCT or AC/ACT) interface design, which is covered in AnswerFAX document number 7001, "System Design". See Section 8, "How to Use AnswerFAX".

TABLE 4. OUTPUT DRIVE CURRENT FOR 74FCT

DEVICE NUMBER	l _{OH} (mA)	I _{OL} (mA)
74FCT240	15	64
74FCT241	15	64
74FCT244	15	64
74FCT245	15	64
74FCT273	15	48
74FCT373	15	48
74FCT374	15	48
74FCT533	15	48
74FCT540	15	64
74FCT541	15	64
74FCT543	15	64
74FCT564	15	48
74FCT573	15	48
74FCT574	15	48
74FCT623	15	64
74FCT646	15	64
74FCT651	15	64
74FCT652	15	64
74FCT653	15	64
74FCT654	15	64
74FCT821A-824A	15	48
74FCT841A-844A	15	48
74FCT861A	15	48
74FCT863A	15	48
74FCT2952A	15	64
74FCT7623	15	64

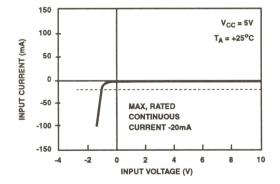


FIGURE 15. FCT INPUT CHARACTERISTIC

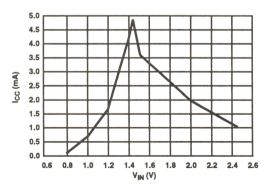


FIGURE 16. SUPPLY CURRENT VS INPUT VOLTAGE FOR FCT (TYPICAL)

Shown in Figure 19A is the FCT test circuit. A Thevenin equivalent may be used for output loading.

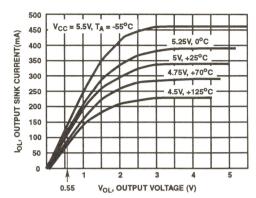


FIGURE 17. OUTPUT SINK CURRENT VS OUTPUT VOLTAGE FOR FCT

TABLE 5. VOH FOR CMOS LOADS; IOH = 1µA

V _{CC} (V)	T _A (°C)	V _{OH} (V)
4.50	+125	3.5
4.75	+70	3.7
5.00	+25	4.0
5.25	0	4.2
5.50	-55	4.4

NOTE: See Figure 18.

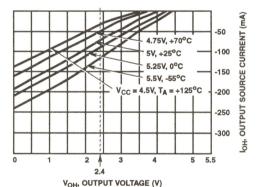


FIGURE 18. OUTPUT SOURCE CURRENT vs OUTPUT VOLTAGE
FOR FCT

Dynamic Characteristics

Switching Speed

Since FCT is a low-power drop-in replacement for Fairchild Advanced Schottky TTL (FAST) 8-bit, 9-bit and 10-bit devices, the propagation delay specifications are set to equal those of the FAST family. As such, FCTXXX/A is generally the same speed as the Advanced CMOS Logic (AC/ACT) family, which should be considered a complementary,

rather than competing, family. FCTXXXAT, however, is an average of 30% faster than either FAST or AC/ACT, thus creating a new speed standard that bipolar TTL cannot match. To keep switching noise under control and meet FCC emission specifications while using these extremely fast ICs, the system designer should employ transmission-line terminations, superior decoupling, and careful PC board layout.

The speed of an octal interface IC is usually characterized by the propagation delay on a single channel. For example, the CD74FCT240 Octal Inverting Buffer/Line Driver is specified for a maximum t_{PHI} and t_{PIH} of 8.0ns when operating in an ambient temperature (TA) between 0°C and +70°C. It should be noted that all FCT specifications apply to both output signal transition directions: LH/HL, ZH/ZL, and LZ/HZ, whereas FAST frequently specifies widely different t_{PLH} and t_{PHL} values. Most designers will have to use the slower of the two values in their designs. Switching-speed parameters for FCT device types match those of JEDEC standard No. 18. Harris FCT ICs are offered for two temperature ranges: commercial 74 series (0°C to +70°C) and military/extended industrial 54 series (-55°C to +125°C) and are tested against the corresponding AC parameters. Thus, while a 74 series part will operate over the full extended range, it is not guaranteed to meet 54 series AC parameter specifications over the full range. Figure 19 depicts the JEDEC standard for the switching-speed test circuit and timing waveform definitions. These are the same that are used for FAST and AS; but differ slightly from those used to test AC/ACT.

FCTXXXAT - Higher Speed Version

Harris offers FCT products in two speed grades: Base speed and higher speed. The base speed version of each type is designated as either FCTXXX or FCTXXXA (the latter for 800 or 2900 series types). The higher speed versions are designated as FCTXXXAT when the base version is FCTXXX. The "T" serves to emphasize the fact that Harris FCT devices provide a TTL-like output swing, thereby reducing ground bounce. (The Harris base speed versions also offer this feature, but since those parts and numbers have already been established, they will not be changed.) Some examples:

BASE FCT PRODUCT	HIGHER SPEED PRODUCT
CD54/74FCT245E	CD54/74FCT245ATE
CD54/74FCT245M	CD54/74FCT245ATM

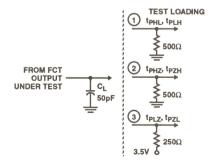
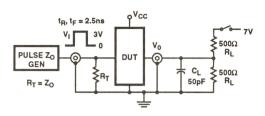


FIGURE 20. HARRIS (AND JEDEC) FCT TEST LOAD CIRCUITS

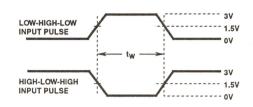


TEST	SWITCH POSITION
t _{PLZ} t _{PZL} Open Drain	Closed
[†] РНZ [†] РZН [†] РLН [†] РНL	Open

NOTES:

- 1. C_L = Load capacitance includes jig and probe capacitance.
- 2. R_T = Termination should be equal to Z_{OUT} of the pulse generator. (Typ. 50Ω).
- 3. $V_{IN} = 0V \text{ to } 3V$.
- 4. Input: $t_R = t_F = 2.5$ ns (10% to 90%), unless otherwise specified.

FIGURE 19A. TEST CIRCUIT



OUTPUT REQUIREMENTS

- Device must follow truth table.
 V_{OL} ≤ 0.55V
 - V_{OH} ≥ 2.4V
- 2. Input Conditions:
- $t_R = t_F \le 2.5$ ns (as fast as required)
- 3. Standard Output Loading:
 - $R_L = 500\Omega$
 - $C_L = 50pF$

FIGURE 19B. INPUT PULSE WIDTH

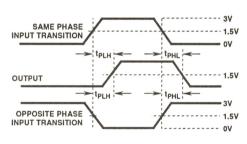


FIGURE 19C. PROPAGATION DELAY TIMES

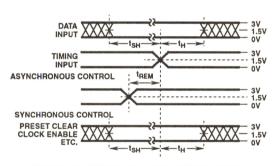


FIGURE 19D. SETUP, HOLD AND REMOVAL TIMES

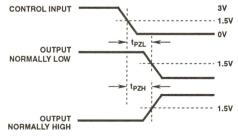


FIGURE 19E. OUTPUT ENABLE TIMES

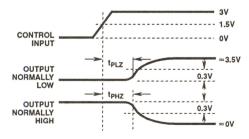


FIGURE 19F. OUTPUT DISABLE TIMES

FIGURE 19. TEST CIRCUIT AND TIMING DEFINITIONS FOR FCT

Harris FCTXXXAT high speed versions are, on the average, 30% faster than either FCT or FAST. Speeds are also faster than the AS, BCT, or BC bus interface families.

Speed vs Capacitive Load

Propagation delays for FCT interface types are determined using a JEDEC standard load as shown in Figure 20. The 50pF capacitor approximates a fan-out of 5-10 CMOS/TTL loads, which is reasonable for on-board operation, but probably too low for bus-interface applications. Figure 21 illustrates the effect of different capacitive loads on propagation delays. Above $C_L = 50pF$ the delta delay is about 16ps/pF.

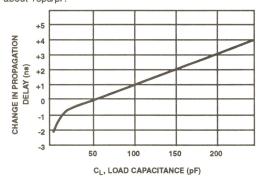


FIGURE 21. CHANGE IN PROPAGATION DELAY AS A FUNCTION OF LOAD CAPACITANCE FOR FCT

Propagation Delay vs Temperature and V_{CC}

The active delay and the delays caused by enabling and disabling outputs are plotted in Figure 22. Parameters $t_{PLH},\, t_{PLZ},\, t_{PZL},\, t_{PHZ},\, t_{PZH}$ are shown as they vary over the temperature range of -55°C through +125°C and over the V_{CC} range of 4.50V to 5.50V. Mean data is for the FCT244 non-inverting buffer function.

Min/Max Delay Issue and Solution

Figure 23 vividly illustrates the wide Min/Max delay spread of FCT data sheet (D/S) specifications. It is readily seen that for the 74FCT373 part the design engineer would unhappily use a Min delay of 1.5ns and a Max delay of 8.0ns. This infers that for any two 373 octal latches making up a 16-bit-wide bus-interface, 8 bits could traverse the IC at 1.5ns while the other 8 bits take 8.0ns! This is a significant spread and can limit useful system clock frequency.

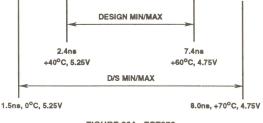
However, by making two simple adjustments to the Min/Max delays, a tighter set of useful design Min/Max delays are obtained:

- Adjust ±0.5ns for built-in guardbands used for test correlation of ICs, not design use.
- Adjust for temperatures greater than 0°C and less than +70°C.

Rules for Useful Design Min/Max

- 1. $t_P Min = D/S Min + 0.5ns + 0.01ns/{}^{\circ}C$
- 2. tp Max = D/S Max 0.5ns 0.01ns/°C

These rules are applicable to t_{PLH} , t_{PHL} , t_{PZL} , t_{PZL} , t_{PZH} , t_{PH2} . In Figure 23A, the D/S and design values are shown; certainly a Min/Max range of 2.4ns to 7.4ns for a PCB operating at $+50^{\circ}\text{C} \pm 10^{\circ}\text{C}$ is more useful than 1.5ns to 8.0ns.



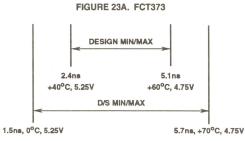


FIGURE 23B. FCT373AT

FIGURE 23. EXAMPLE SHOWING DESIGN VALUES VS DATA SHEET VALUES FOR MIN/MAX DELAYS

Even more beneficial is application of the higher speed suffix "AT" FCT parts. As shown in Figure 23B, the design Min/Max spread is only 2.4ns to 5.1ns; this is very useful! The two design rules for Min/Max are applicable to all Harris FCT types.

Delay Skew

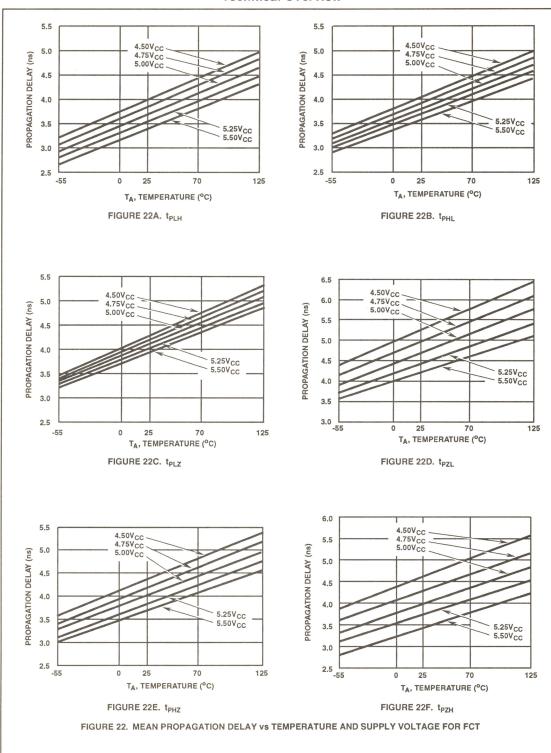
Each 8-bit, 9-bit and 10-bit part will have propagation delay skews that fall into three categories:

- Pin to pin skew
- · Simultaneous switching skew
- H-L vs L-H (edge) skew

Table 6 records the skew data for the three categories. Simultaneous switching skew is measured with 7/8 outputs switching rather than 8/8 due to the immediate availability of a good RF ground bounce fixture. Skew would be slightly larger for 8/8 switching. The largest incremental delay change occurs for 7/8 outputs switching H-L. The incremental change for the H-L skew is larger than that for the L-H skew due to output edge control circuitry.

Dynamics of Ground Bounce

Octal or 9/10-Bit bus-interface parts, when switching simultaneously, will have worst-case noise glitches on otherwise quiet outputs when N-1 of the N outputs all go HIGH or LOW at the same instant. In a practical sense, skew of the IC channels (up to 1ns) and skew of PCB interconnection (possibly 0.5ns to 1ns) will cause outputs to switch at slightly different times; therefore, this is a "Murphy's Law" exercise what if all 7 outputs of an FCT octal (such as the popular 245



transceiver or the 373 latch) all switch H-L or L-H on top of each other? Figure 24A and Figure 24B show the ground bounce ($V_{\rm OLP}$) noise glitch for Harris FCT245 and 373 types and Figure 24C shows the $V_{\rm CC}$ bounce ($V_{\rm OHV}$) glitch for the FCT373 type - all very representative of the Harris IC and package design for minimized switching noise. In fact, the FCT373 devices used for these measurements operate at "AT" speed. Figure 25 shows the measured ground bounce of a competitor's FCT 245 IC. Ground bounce measurements for the competitor's FCT 245A are even higher. Application Note AN9001 provides a detailed description of Harris accurate Ground/ $V_{\rm CC}$ Bounce Test PCBs and how readers may obtain one for their own measurements. From the waveforms in Figure 24 and Figure 25, a summary of useful observations is shown in Table 7.

TABLE 6. TYPICAL PROPAGATION DELAY SKEW FOR THE FCT245

		PROPAGATION DELAY (ns)					
оит	PUT	1/8 SWITCHING		SWIT (/8 CHING	INCREMENT 1/8 TO 7/8	
PIN#	NAME	t _{PHL}	t _{PLH}	t _{PHL}	t _{PLH}	t _{PHL}	t _{PLH}
11	B7	5.19	5.09	6.32	5.68	1.13	0.59
12	B6	5.06	4.76	6.40	5.64	1.34	0.88
13	B5	5.14	4.75	6.40	5.60	1.26	0.85
14	B4	4.93	4.82	6.40	5.56	1.47	0.74
15	В3	5.12	4.78	6.40	5.56	1.28	0.78
16	B2	5.30	4.86	6.40	5.24	1.10	0.38
17	B1	5.22	4.86	6.40	5.24	1.18	0.38
18	B0	5.25	4.84	Quiet	Quiet	-	-
Pin to Pin Skew		0.37	0.34	0.08	0.44	-	-
Maximum Edge Skew		0.	44	1.	16	-	
Maximum 1/8 to 7/8 Skew		-	-	-	-	1.	47

NOTE: $V_{CC} = 5V$, $T_A = +25^{\circ}C$.

TABLE 7. SELECTED DATA FROM FIGURE 24 AND FIGURE 25

DEVICE TYPE	V _{OLP} (V)	UNDER SHOOT (V)	PULSE WIDTH AT 0.8V (ns)	V _{OHV} (V)
Harris FCT245/AT	1.24	0.83	3.0	
Harris FCT373/AT	1.24	0.9	3.5	0.46
Competitive FCT245	2.00	0.85	3.0	-
Second Peak	1.1	-	3.0	-

NOTES:

- 1. V_{OLP} exceeds D/S V_{IL} of 0.8V in all cases. Even the second peak of the competitive 245 ground bounce ringing waveform exceeds this limit.
- Widths are under 3.5ns at 0.8V. This means that a wait time to strobe an output would be no longer than about 4ns after outputs switch H-L.
- 3. The one-of-seven switching outputs that is monitored for the Harris FCT device shows minimal undershoot and overshoot illustrating benefits of designed-in ground/V_{CC} bounce minimization techniques. However, competitive H-L active output undershoots by 1.5V and falls faster illustrating the lack of a slowing H-L edge control.

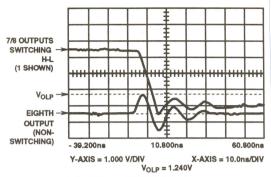


FIGURE 24A. HARRIS 245 - VOLD

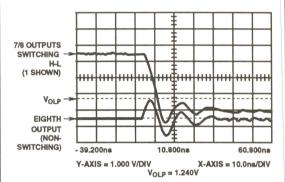


FIGURE 24B. HARRIS 373 - VOLP

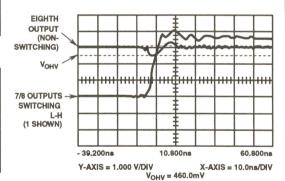


FIGURE 24C. HARRIS 373 - VOHV

FIGURE 24. GROUND BOUNCE (V_{OLP}) AND V_{CC} BOUNCE (V_{OHV})
FOR HARRIS FCT

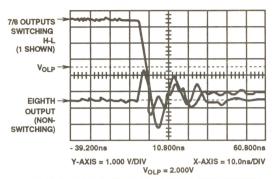


FIGURE 25. GROUND BOUNCE (V_{OLP}) FOR A COMPETITOR'S FCT

System Design Aspects of V_{OLP} and V_{OHV}

Although Harris FCT outputs might produce a peak ground bounce glitch of 1.25V, Harris FCT inputs will not respond. A built-in hysteresis circuit at each input adds about 0.2V to the input switchpoint voltage.

Power Consumption

Operating Current/Power

For Bus-Interface Logic ICs that are specified to match VME, Multibus II or other bus standards, FCT is clearly the lowest current drain family, and hence lowest heat dissipation family. Figure 26 is actual measured current up through 20MHz operation for 7/8 outputs switching into a 50pF load. Since VIH is 3.5V, the ICC component of FCT current drain is included; Figure 26 is a very real-world comparison of bipolar FAST, BiCMOS BCT, and Harris BiCMOS FCT. Results are very obvious for relative current drain; for example at standby (f = 0) FCT current drain is virtually zero while BCT and FAST are at 50mA and 75mA respectively. For a continuous clock, up through 20MHz, both FCT and BCT save power over FAST. Most importantly, for overall average current drain of data or address buffers, at 5MHz, FCT shows over a 2.5X savings in current, and a corresponding savings in power (or heat dissipation) in a system.

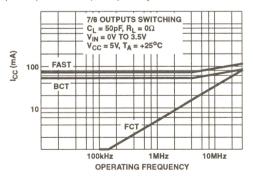


FIGURE 26. OPERATING CURRENT (I_{CC}) AS A FUNCTION OF OPERATING FREQUENCY FOR FAST, BCT, AND HARRIS FCT

Even for the Hi-Z mode, when outputs hanging on a bus are disabled, FCT saves 188X in standby or Hi-Z IC power consumption.

TABLE 8. FCT vs BCT POWER DISSIPATION COMPARISON

	I _{CC} MAXIMUM	POWER MAXIMUM
FCT	0.08mA	0.44mW
BCT	15mA	82.5mW

NOTE: V_{CC} = 5.5V, T_A = +70°C, Outputs Hi-Z, Data Sheet Values.

Power Estimating

The system designer needs to get a good handle on his PCB power consumption in order to specify his power supply, design for thermal control, and also to estimate decoupling capacitor sizes and ferrite bead currents for EMI control. Equation 2 shows the exact FCT power consumption equation per IC input or per IC function. Without going through the data sheets to extract parameters to put into this equation let's look at a concise set of values applicable to all Harris FCT types:

TABLE 9. PARAMETERS FOR CALCULATING POWER CONSUMPTION

PARAMETERS	TYPICAL V _{CC} = 5V T _A = +25°C	MAXIMUM V _{CC} = 5.5V T _A = +70°C	MAXIMUM V _{CC} = 5.5V T _A = +125°C
Icc	0	80μΑ	500μΑ
ΔI _{CC}	0.4mA	1.6mA	2mA
C _{PD} (Note 1)	40pF	60pF	60pF

NOTE: 1. Will vary somewhat with device type.

All other variables such as C_L per output, and input/output frequencies are estimates made by the system designer, remembering that average frequency (not peak) is used for power averaging.

$$P = I_{CC} \ V_{CC} \underbrace{+ \Delta I_{CC} \ V_{CC} D + C_{PD} V_{CC} \ ^2 f_i}_{Per \ Input/Function} \underbrace{+ C_L (V_{CC} - 1.4V)^2 f_O}_{Per \ Output/Function} (EQ. \ 2)$$

Where:

I_{CC} = Quiescent Current (From Data Sheet Ratings)

V_{CC} = Supply Voltage

f_i = Input Frequency

fo = Output Frequency

C_{PD} = Device Equivalent Power Dissipation Capacitance; Used for Computing Internal Chip Power ≈ 40pF

 $\mathrm{C_L} = \mathrm{Load}$ Capacitance; Used for Computing Output Stage Power

 ΔI_{CC} = Added Direct Current When V_{IN} = V_{CC} -2.1V (TTL Input High Level)

D = Duty Cycle of Input (Percent of Time High)

System Design Considerations

System Design Using Harris FCT

Successful system design using Harris FCT is assured if the fundamental DC drive and major speed considerations already covered are understood - and if "Golden Rules" of Design and PCB layout are followed. It is not enough simply to apply the static and dynamic characteristics in order to achieve excellent fault-free computer system operation, the system design engineer must also approach his hardware design task so as to stay within stringent EMI limits for conducted and radiated energy.

Ten Golden Rules for Successful Design with FCT

- No Floating Inputs Tie unused inputs to GND or V_{CC}. For transceiver I/O pins, return floating inputs to V_{CC} or ground via a resistor (100Ω or more) to avoid output shorts.
- Decouple Each IC Correctly Decoupling differs for data (non-periodic) signal ICs and clock (or periodic signal) ICs.
 - A. Data/Address (non-periodic) Place a decoupling capacitor with value C_D on same side of PCB as IC with shortest possible leads to V_{CC} and ground pins. Given a choice, put C_D closer to V_{CC} pin to minimize EMI on power buses. Placing C_D on the opposite side of the board is not as effective.

$$C_D = 9 N C_{PD} + 9 \sum_{1}^{N} C_L$$
 EQ. 3

N = Number of Functions in IC

Also specify C_D to have:

ESL < 10nH

 $ESR < 0.5\Omega$

- B. Clock Generator and Driver ICs (Periodic Signals) -20MHz to 40MHz periodic clocks, strobes, etc. have harmonics in the EMI band (150MHz and up) where FCC rules are stringent. Decouple periodic signal ICs with both a C_D and ferrite bead. Combination three terminal devices for this purpose are available (the Murata Erie DS 310 types, for example). Place on same side of PCB as IC.
- 3. Terminate Interconnects More than Six Inches in Length-VME, Multibus II, and other bus standards specify adequate Thevenin termination. Interconnects within a PCB may not need to be terminated but should be if they are six inches or more in length. This avoids reflection problems and also avoids crosstalk problems should two parallel PCB traces run alongside each other for six inches or more. A termination also keeps ground bounce noise glitches from increasing in amplitude much over 1.25V, thereby preventing these glitches from false triggering inputs.
 - Terminations may be series, shunt, or Thevenin.
- 4. Low-Voltage Operation While Harris FCT may be operated below 4.5V, it was not designed for this purpose. Harris AC logic, operable down to $V_{\rm CC}=1.5{\rm V}$ is recommended for battery operation or battery backup. (References 5 and 6).

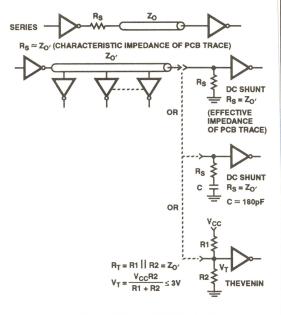


FIGURE 27. METHODS OF TERMINATION

- 5. Live PCB Insertion and Multi-System Interfacing is Safe With Harris FCT - Because Harris FCT (unlike other FCT) does not have input or output clamp diodes to V_{CC} there is no danger in live insertion of PCB with Harris FCT as buffers. With other buffers, live bus clocks or data can momentarily be loaded down causing loss of information. This problem will not occur with Harris FCT. Also interfacing between two systems having different power sources is facilitated.
- Momentarily Shorting Outputs is Allowed But Restricted-If forced node testing is done, please be careful not to overheat the FCT IC (short only one output pin per package, for no more than 1s).
- 7. Interfacing FCT to Other Logic Families Harris FCT Bus-Interface ICs interface easily to all other CMOS, Bipolar, and BiCMOS logic families directly as shown in Table 10. Note 1 applies to the interface between FCT devices and those that have CMOS switching levels (HC or AC); the only limitation is a reduced noise margin from what it would be if FCT had a full 5V swing. Harris FCT is intentionally designed to provide a reduced output swing. The user should understand that not swinging to 5V has overwhelming advantages, namely:
 - A. Less crosstalk jeopardy
 - B. Less switching noise, i.e. lower ground/V_{CC} bounce
 - C. Less radiated and conducted EMI

TABLE 10. INTERFACING FCT AND OTHER LOGIC FAMILIES

		то						
FROM	FCT	HCT/ ACT	HC/AC	FAST AS ALS/LS	BC/FCT			
FCT	Direct	Direct	Direct (Note 1)	Direct	Direct			
AC/ACT	Direct	Direct	Direct	Direct	Direct			
HC/HCT	Direct	Direct	Direct	Direct	Direct			
FAST AS/ALS/LS	Direct	Direct	(Note 2)	Direct	Direct			
BC/BCT	Direct	Direct	(Note 2)	Direct	Direct			

NOTES:

- For Harris FCT to HC or AC logic families, the low logic level noise margin is 1.4V (V_{OL} < 0.1V and V_{IL}Max = 1.5V). The high logic level noise margin is as shown in Table 11.
- 2. For any of the TTL families (FAST, AS, ALS, LS) or the BC, BCT BiCMOS families, for low logic levels (V_{OL} to V_{IL}) there is a good noise margin of at least 1.2V. For high logic levels (V_{OH} to V_{IH}) the noise margin varies with family. If the manufacturer does not supply data like that shown in Table 11 for Harris FCT, then a pull-up resistor to V_{CG} at the interface is necessary.
- 8. Avoid Crosstalk Problems As shown in Figure 28, if two PCB interconnect copper traces on the same layer run closely spaced in parallel for enough distance (L) without terminations, a noise glitch at B can be large enough to switch that input. Rules to avoid problematic crosstalk:
 - A. For FCT keep L conservatively under six inches if runs have to be paralleled.
 - B. If parallel runs exceed six inches, terminate with $R_S = Z_0$ of trace. Place a C of about 180pF in series with R_S to reduce power. Also a ground trace could be placed between runs.
 - C. Best bet is to avoid parallel runs of over six inches. Use different PCB levels separated by a V_{CC} or ground plane.

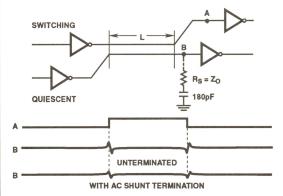
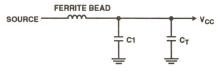


FIGURE 28. SIGNAL CROSSTALK RESULTS FROM PARALLEL
TRACES AND IS REDUCED BY TERMINATION

- Ground/V_{CC} Bounce Will Not Affect Performance with These Simple Rules:
 - A. V_{CC} bounce is under 0.5V; usually not a problem.
 - B. Ground bounce is about 1.25V, about half of that of competitive FCT, but above V_{IL}Max of 0.8V. Even though Harris FCT ground bounce is well below the input switchpoint, particularly with sufficient pulse width to false trigger an input, other system noise and/or DC offset of 0.2V to 0.3V above ground due to high DC loading could false trigger an input if the line is not terminated. Therefore, if an output with a potential for ground bounce exists, terminate with either series or shunt RS as described in Rule 3 above. Remember, an unterminated line produces a signal of 2X amplitude at the end of the unterminated trace. This could easily cause false triggering. If ground bounce occurs at latch or flip-flop data inputs, its 3ns width at 0.8V and its centering right at the output edge (See Figure 24) is such that no extra strobe delay or system clock frequency reduction is needed.

Because FCT inputs have typically 200mV of hysteresis, input dynamic noise margin remains above 0.5V in the presence of ground bouncing, i.e. internal stored data is not subject to loss for Harris FCT; this is a problem in competitive FCT which has 2V or more of ground bounce!

- 10. PCB Must Be Designed to Minimize EMI Before initiation of the PCB layout and design, it is imperative that a comprehensive action plan to minimize EMI be put into place realizing that high speed digital ICs are EMI spectrum generators. Whether it is FCT, AC/ACT, FAST, VLSI, ASICs or memory, with clock rates above 10MHz and switching edges below 5ns, PCB design for EMI containment will pay off in the end designers will not have to apply painful "band-aids", or worse scrap the PCB design, after equipment is built. Guidelines for EMI control in PCB application of FCT or like devices follow:
 - A. Become familiar with EMI control measures There are good comprehensive text books and reports available on PCB design spanning layout, decoupling, board materials, terminations, shielding, grounding, etc. Some of these are listed as references at the end of this section. Tutorial seminars are available from sources such as The Keenan Corporation listed as a reference. Absolute musts are summarized in the following notes.
 - B. Decouple carefully.
 - 1. ICs as described in Rule 2 above.
 - 2. PCB power entry each power plane area on PCB



 $C1 = 0.1 \mu F RF CAPACITOR$

C_{TMIN} = TANTALUM CAPACITOR EQUAL TO SUM OF ALL DECOUPLING CAPACITORS ON BOARD

FIGURE 29. DECOUPLING CAPACITORS AT POWER ENTRY POINT ON PC BOARD

TABLE 11. NOISE MARGINS FOR INTERFACING HARRIS FCT TO AC OR HC LOGIC

	FCT OUTPUT VOLTAGE			AC OR HC IN	NOISE MARGIN			
LOW LOGIC LEVEL		V _{OL} < 0.1V		V _{IL} = 1.5\	/ MAXIMUM	1.4V		
HIGH LOGIC LEVEL	V _{OH} (V)			Vi	V _{IH} (V)			
	V _{CC} (V)	T _A (°C)	V _{OH} (V)	MINIMUM SPECIFIED	ACTUAL SWITCHING VOLTAGE	MINIMUM	ACTUAL	
	4.50	+125	3.5	3.15	1.90 to 2.60	0.35	0.90	
	4.75	+70	3.7	3.33	2.03 to 2.73	0.37	0.97	
	5.00	+25	4.0	3.50	2.15 to 2.85	0.50	1.15	
	5.25	0	4.2	3.68	2.28 to 2.98	0.52	1.22	
	5.50	-55	4.4	3.85	2.40 to 3.10	0.55	1.30	

- C. Isolate IC block with separated power planes On a multi-layer PCB (preferred over two-sided) use a separated V_{CC} plane for various system blocks such as high speed synchronous logic, I/O logic, memory, lower-speed logic, analog circuits. For each segmented V_{CC} area use separate power entry decoupling as illustrated in Figure 29.
- D. Periodic Signal Buffers, Main Culprit As discussed, take special care in decoupling, terminating, grouping, and laying out short ground return paths. It has been found^[1-4] that most out-of-specification EMI frequency peaks are harmonics of periodic signals, and can be traced back to a violation of the "Golden Rules" covering periodic signals in the design of PCBs.
- E. IC Placement FCT as PCB I/O should be very close to the connector with its isolated V_{CC} plane. This minimizes the inductance of high current V_{CC} and ground paths. Group synchronous clocked logic and micros closely, again with a dedicated V_{CC} plane in an area close to PCB connector but secondary to I/O. Slower speed and/or asynchronous logic should be grouped in a separate area with its own V_{CC} plane, and can be farther from connector. Likewise analog signal ICs must have separate V_{CC} and ground planes providing separate power entry.
- F. Terminate Terminations always reduce ringing on a PCB interconnect at FCT-like speed. Follow guidance of Rule 3 above.

References

- Harris Semiconductor, Application Note AN8906, "Noise Aspects of Applying Advanced CMOS (AC/ACT) Semiconductors," April 1989.
- [2] R. Kenneth Keenan, "Decoupling and Layout of Digital Printed Circuits," The Keenan Corporation, Pinellas Park, FL.
- [3] R. Kenneth Keenan, "Digital Design for Interference Specifications," The Keenan Corporation, Pinellas Park, FL.
- [4] The Keenan Corporation, FCC Emissions and Power Bus Noise - 2nd Edition.
- [5] Harris Semiconductor, Data Book SSD-283A, Advanced CMOS Logic ICs. October 1988.
- [6] Nadolski, J. "Logic Designs for Battery-Powered or Battery Backed-Up Operation," Harris Semiconductor Application Note AN7373.
- [7] JEDEC Standard No. 20, "Standard for Description of 54/ 74ACXXXX and 54/74ACTXXXX Advanced High Speed CMOS Devices".
- [8] JEDEC Standard No. 18, "Standard for Description of 54/ 74FCTXXXX High Speed CMOS[/BiCMOS] Devices".

Absolute Maximum Ratings

DC Supply Voltage, V _{CC} 0.5 to +6V DC Input Diode Current, I _{IIK}
For V ₁ < -0.5V20mA
DC Output Diode Current, IOK
For V _O < -0.5V50mA
DC Output Sink Current Per Output Pin, I _O +70mA
DC Output Source Current Per Output Pin, Io30mA
DC V_{CC} , Current, I_{CC} $N(I_{OH}) + M(\Delta I_{CC})mA$
DC Ground Current, I_{GND} $N(I_{OL}) + M(\Delta I_{CC})mA$
Where N = No. of Outputs
M = No. of Inputs

Maximum Power Dissipation per Package, PD	
Package E, EN	
$T_A = -55^{\circ}C \text{ to } +100^{\circ}C$	00mW
T _A = +100°C to +125°C Derate Linearly at 8mW/°C to 3	00mW
Package M	
$T_A = -55^{\circ}C \text{ to } +70^{\circ}C$	00mW
T _A = +70°C to +125°C Derate Linearly at 6mW/°C to	70mW
Operating Temperature Range, TA55°C to 4	-125°C
Storage Temperature, T _{STG} 65°C to 4	-150°C

Lead Temperature (During Soldering) At Distance 1/16in. ± 1/32in. (1.59mm ± 0.79mm)

From Case for 10s Max +265°C Unit Inserted into a PC Board (Min Thickness 1/16in. or 1.59mm) with Solder Contacting Lead Tips Only +300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Supply - Voltage Range V _{CC} (Note 1)	Operating Temperature Range, T _A 55°C to +125°C
T _A = 0°C to +70°C (74 Series)	DC Input or Output Voltage, V _I , V _O 0V to V _{CC}
$T_A = -55^{\circ}\text{C to } +125^{\circ}\text{C } (54 \text{ Series}) \dots4.5V to 5.5V$	Input Rise and Fall Slew Rate, dt/dv 0ns/V to 10ns/V

DC Electrical Specifications For FCT Series, 74FCT Commercial Temperature Range, 0°C to +70°C, V_{CC} = 4.75V Min to 5.25V Max For 54FCT Extended Industrial Temperature Range, -55°C to +125°C, V_{CC} = 4.5V Min to 5.5V Max

		TEST CONDITIONS		V _{cc}	+25	°C	0°C TO	+70°C	-55°C +125		
PARAMETERS	SYMBOL	V _I (V)	l _O (mA)	(V)	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	2	-	2	-	٧
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High Level Output	V _{OH}	V _{IH} or V _{IL}	-15 (Note 4)	Min	2.4	-	2.4	-	-	-	٧
Voltage			-12 (Note 4)	Min	2.4	-	-	-	2.4	-	٧
Low Level Output Voltage	V _{OL}	V _{IH} or V _{IL}	64 (Note 4)	Min	-	0.55	-	0.55	-	-	٧
			48 (Note 4)	Min	-	0.55	-	-	-	0.55	٧
High Level Input Current	I _{IH}	V _{cc}	-	Max	-	0.1	-	1	-	1	μА
Low Level Input Current	I _{IL}	GND	-	Max	-	-0.1	-	-1	-	-1	μА
Three-State Leakage	l _{ozh}	V _{cc}	-	Max	-	0.5	-	10	-	10	μА
Current	I _{OZL}	GND	-	Max	-	-0.5	-	-10	-	-10	μА
Short Circuit Output Current (Note 2)	los	V _{CC} or GND V _O = 0	-	Max	-60 (Note 4)	-	-60 (Note 4)	-	60 (Note 4)	-	mA
Input Clamp Voltage	V _{IK}	V _{CC} or GND	-18	Min	-	-1.2	-	-1.2	-	-1.2	٧
Quiescent Supply Current	Icc	V _{CC} or GND	0	Max	-	8	-	80	-	500	μА
Additional Quiescent Supply Current per Input Pin, TTL Inputs High, 1 Unit Load	Δl _{CC}	3.4 (Note 3)	-	Max	-	1.6	-	1.6		2	mA

NOTES:

- 1. Unless otherwise specified, all voltages are referenced to GND.
- 2. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
- 3. Inputs that are not measured are at V_{CC} or GND. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Chart, e.g., 1.6mA Max at +70°C.
- 4. Values are for FCT240 types (See Table 4 for I_{OL} and I_{OH} for other types).

For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX. See Section 8, "How to use AnswerFAX", in this selection guide.

Operating and Handling Considerations

Handling

All inputs and outputs of Harris CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in AN6525. "Guide to Better Handling and Operation of CMOS Integrated Circuits."

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{CC} - GND to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{CC} nor less than GND. Input currents must not exceed 20mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or GND, whichever is appropriate.

Output Short Circuits

Shorting of outputs to $V_{\rm CC}$ or GND may damage CMOS devices by exceeding the maximum device dissipation.

Substrate Connection

When devices in chip form are used in hybrid applications, the substrate is connected to GND (as with all P-substrate devices).

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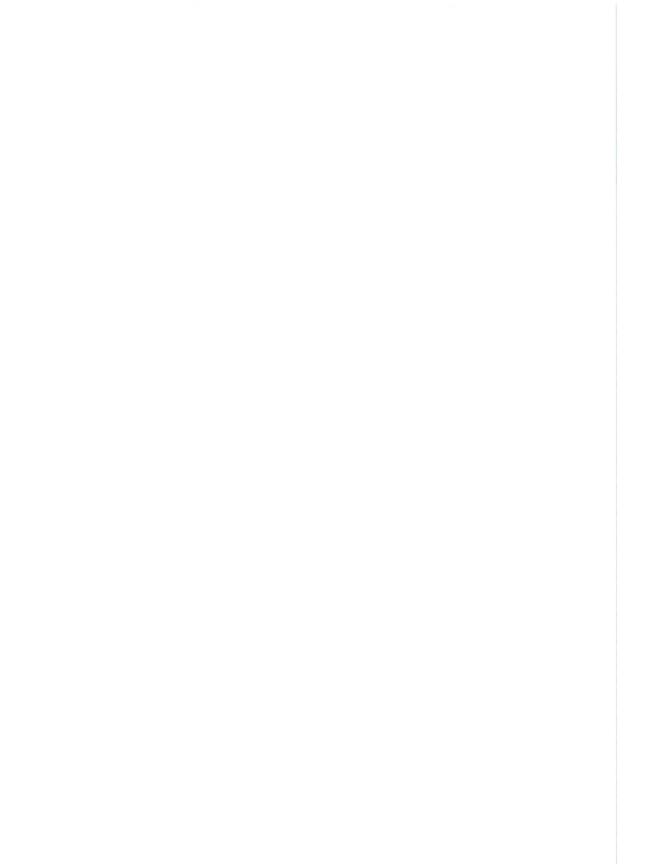
D4000B SERIES

CMOS LOGIC ICs

PRODUCT SELECTION GUIDE

CMOS LOGIC - CD4000B SERIES

	PAGE
TECHNICAL OVERVIEW	5-3
CD4000B Series.	5-3
General Operating and Handling Considerations	5-3
High Voltage B-Series CMOS Integrated Circuits.	5-7
FAMILY RATINGS AND SPECIFICATIONS‡	5-12
ENHANCED PRODUCT	5-18



CD4000B Series

This section is intended as a guide for circuit and equipment designers in the operation and application of MOS integrated circuits. It covers general operating and handling considerations with respect to the following critical factors:

- · Operating Supply Voltage Range
- · Power Dissipation and Derating
- · System Noise Considerations
- Power Source Rules
- · Gate-oxide Protection Networks
- · Input Signals and Ratings
- · Chip Assembly and Storage
- Device Mounting
- Testing

More specific information is then given on significant features, special design and application requirements, and standard ratings and electrical characteristics for CMOS B-series logic circuits, and on CMOS special function circuits (special interface and display driver circuits).

General Operating and Handling Considerations

The following paragraphs discuss some key operating and handling considerations that must be taken into account to achieve maximum advantage of the CMOS technology. Additional information on the operation and handling of CMOS integrated circuits is given in Application Note AN6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits". See Section 8, "How to Use Answer-FAX", in this selection guide.

Operating Supply Voltage Range

Because logic systems occasionally experience transient conditions on the power supply line which, when added to the nominal power-bus voltage, could exceed the safe limits of circuits connected to the power bus, the recommended operating supply voltage range is 3V to 18V for B-series devices. The recommended maximum power supply limit is substantially below the minimum primary breakdown limit for the devices to allow for limited power supply transient and regulation limits. For circuits that operated in a linear mode over a portion of the voltage range, such as RC or crystal oscillators, a minimum supply voltage of 4V is recommended.

Power Dissipation and Derating

The power dissipation of a CMOS integrated circuit is the sum of a DC (quiescent) component and an AC (dynamic) components. The DC component is the sum of the net integrated circuit reverse diode junction current and the surface leakage current times the supply voltage. In standard Bseries logic devices, the DC dissipation typically ranges, depending upon device complexity, from 100nW to 400nW for a supply voltage of 10V. Worst-case DC dissipation is the product of the maximum quiescent current (given in the data sheet on each device) and the DC supply voltage VDD.

Dynamic power dissipation has three components:

- The dissipation that results from current that charges and discharges the external load capacitance of the output buffers. The dissipation of each output buffer is equal to CV²f, where C is the load capacitance, V is the supply voltage, and f is the switching frequency of that output.
- 2. The dissipation that results from current that charges and discharges the internal node capacitances.
- The dissipation caused by the current spikes through the PMOS and NMOS transistors in series at the instant of switching. This component amounts to approximately 10% of the total dissipation, shown graphically in the datasheets of most CMOS circuits.

All CMOS devices are rated at 200mW per package at the maximum operating ambient temperature rating (T_A) of 125°C for all packages. Power ratings for temperatures below the maximum operating temperature are shown in the standard CMOS thermal derating chart in Figure 1. This chart assumes that the device is mounted and soldered (or placed in a socket) on a PC board; there is natural convection cooling, with the PC board mounted horizontally; and the pressure is standard (14.7psia). In addition to the overall package dissipation, device dissipation per output transistor is limited to 100mW maximum over the full package operating temperature range.

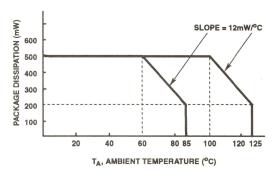


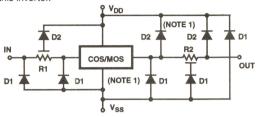
FIGURE 1. STANDARD CMOS THERMAL DERATING CHART

System Noise Considerations

In general, CMOS devices are much less sensitive to noise on power and ground lines than bipolar logic families (such as TTL or DTL). However, this sensitivity varies as a function of the power supply voltage, and more importantly as a function of synchronism between noise spikes and input transitions. Good power distribution in digital systems requires that the power bus have a low dynamic impedance; for this purpose, discrete decoupling capacitors should be distributed across the power bus. A more detailed discussion of CMOS noise immunity is provided by Application Note AN6587, "Noise Immunity of B-series CMOS Integrated Circuits". See Section 8, "How to Use AnswerFAX", in this selection guide.

Power Source Rules

Figure 2 shows the basic CMOS inverter and its gate-oxide protection network plus inherent diodes. The safe operating procedures listed below can be understood by reference to this inverter.



NOTES:

- 1. These Diodes are inherently part of the manufacturing process.
- 2. Diode Breakdown

D1 ≈ 25V

D2 ≈ 50V

R2 << R1

FIGURE 2. BASIC CMOS INVERTER WITH B-SERIES TYPE PROTECTION NETWORK

- 1. When separate power supplies are used for the CMOS device and for the device inputs, the device power supply should always be turned on before the independent input signal sources, and the input signals should be turned off before the power supply is turned off (V_{SS} ≤ V_I ≤ V_{DD} as a maximum limit). This rule will prevent over dissipation and possible damage to the D2 input protection diode when the device power supply is grounded. When the device power supply is grounded. When the device power supply is an open circuit, violation of this rule can result in undesired circuit operation although device damage should not result: AC inputs can be rectified by diode D2 to act as a power supply.
- The power supply operating voltage should be kept safely below the absolute maximum supply rating, as indicated previously.
- 3. The power supply polarity for CMOS circuits should not be reversed. The positive (V_{DD}) terminal should never be more than 0.5V negative with respect to the negative (V_{SS}) terminal (V_{DD} V_{SS} > -0.5V). Reversal of polarities will forward-bias and short the structural and protection diode between V_{DD} and V_{SS} .
- V_{DD} should be equal to or greater than V_{CC} for CMOS buffers which have two power supplies (except for the CD40109B, and in particular, for CD4009 and CD4010 CMOS-to-TTL "down" conversion devices).
- Power source current capability should be limited to as low a value as reasonable to assure good logic operation.
- Large values of resistors in series with V_{DD} or V_{SS} should be avoided; transient turn-on of input protection diodes can result from drops across such resistors during switching.

Gate-Oxide Protection Network

A problem occasionally encountered in handling and testing low power semiconductor devices, including MOS and small geometry bipolar devices, has been damage to gate oxide and/or P-N junctions. Figure 3 shows the gate-oxide protection circuits used to protect CMOS devices from static electricity damage. Application Note AN6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits". See Section 8. "How to Use AnswerFAX". in this selection guide.

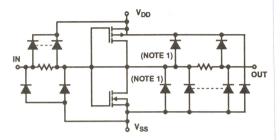


FIGURE 3A. FOR B-SERIES CMOS PRODUCT

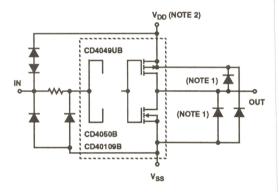


FIGURE 3B. FOR CD4049UB AND CD4050B AND CD40109B CMOS TYPES

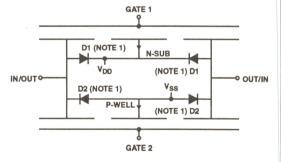


FIGURE 3C. FOR CMOS TRANSMISSION GATES

NOTES:

- 1. These Diodes are inherently part of the manufacturing process.
- 2. V_{CC} for CD4049UB and CD4050B
- 3. Diode Breakdown

D1 ≈ 25V

D2 ≈ 50V

FIGURE 3. GATE-OXIDE PROTECTION NETWORKS USED IN HARRIS CMOS INTEGRATED CIRCUITS

Input Signals and Ratings

Input signals should be maintained with in the power supply voltage range, $V_{SS} \leq V_I \leq V_{DD}.$ If the input signal exceeds the recommended input signal swing range, the input current should be limited to $\pm 100 \mu A$ to minimize cross talk between input signals on adjacent terminals, and also to minimize any reduction in noise immunity.

The absolute maximum input current rating of ± 10 mA, shown in the published data, protects the device against the possible occurrence of an induced V_{DD} - V_{SS} latch condition, or damage to the input protection diodes. Latch-up conditions are explained in Application Note AN6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits". See Section 8, "How to Use AnswerFAX", in this selection guide.

ALL CMOS inputs should be terminated. An exception can be made in the case of unbuffered NOR and NAND gates where terminating one of the series inputs to the proper polarity will not permit current flow caused by a floating input. Thus tying low one of the inputs of an unbuffered NAND gate, or tying high one of the inputs of an unbuffered NOR gate will satisfy this requirement.

When CMOS inputs are wired to edge card connectors with CMOS drive coming from another PC board, a shunt resistor in the range of 100kW should be connected to V_{DD} or V_{SS} , as applicable, in case the inputs become unterminated with the power supply on.

When CMOS circuits are driven by TTL logic, a "pull-up" resistor should be connected from the CMOS input to 5V (further information is given in Application Note AN6602, "Interfacing COS/MOS with Other Logic Families", See Section 8, "How to Use AnswerFAX", in this selection guide.

Output Rules

- The power dissipation in a CMOS package should not exceed the rated value for the ambient temperature specified. The actual dissipation should be calculated when shorting outputs directly to V_{DD} or V_{SS}, driving low impedance loads, or directly driving the base of P-N-P or N-P-N bipolar transistor.
- Output short circuits often result from testing errors or improper board assembly. Shorts on buffer outputs or across power supplies greater than 5V can damage CMOS devices.
- CMOS, like active pull-up TTL, can be connected in the "wire-OR" configuration because an "on" PMOS and an "on" NMOS transistor could be directly shorted across the power supply rails. (Exception: CD40107B)
- Paralleling inputs and outputs of gates is recommended only when the gates are within the same IC package.
- Output loads should return to a voltage within the supply voltage range V_{DD} to V_{SS}.
- Large capacitive loads (greater than 5000pF) on CMOS buffers or high current drivers act like short circuits and may over dissipate output transistors.

Output transistors may be over dissipated by operating buffers as linear amplifiers or using these types as one shot or astable multivibrators.

Noise immunity and Noise Margin

The complementary structure of the inverter, common to all CMOS logic devices, results in a near-ideal input-output transfer characteristic, with switching point midway (45% to 55%) between the 0 and 1 output logic levels. The result is high DC noise immunity.

Figure 4 shows a typical transfer curve that may be used to define the DC noise immunity of CMOS integrated circuits. The noise immunity voltage (V_{IL} or V_{IH}) is the noise voltage at any one input that does not propagate through the system. Minimum noise immunity for buffered B-series CMOS devices is 30%, 30%, and 27%, respectively for supply voltages V_{DD} of 5V, 10V, 15V and 20% of V_{DD} for all unbuffered gates. The V_{IL} and V_{IH} specifications define the maximum permissible additive noise voltage at an input terminal when input signals are within 50mV of the supply rails.

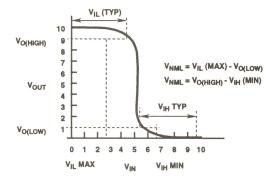


FIGURE 4. TYPICAL TRANSFER CURVE FOR A INVERTING GATE AT $V_{DD} = 10V$

Noise margin is the difference between the noise-immunity voltage ($V_{\rm IL}$ or $V_{\rm IH}$) and the output voltage V_O . Noise margin voltage is the maximum voltage that can be impressed upon an input voltage $V_{\rm IN}$ (where $V_{\rm IN}$ is the $V_{\rm OL}$ or $V_{\rm OH}$ voltage of the preceding stage) at any (or all) logic I/O terminals without upsetting the logic or causing any output to exceed the output voltage (V_O) conditions specified for $V_{\rm IL}$ and $V_{\rm IH}$ ratings. Figure 5 illustrates the noise margin concept in a simple system. Minimum noise margins for buffered B-series CMOS devices are 1V, 2V, and 2.5V, respectively, for supply voltages 5V, 10V, and 15V.

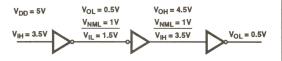


FIGURE 5. NOISE MARGIN EXAMPLE USING INVERTERS

Of the two noise limitation specifications (noise immunity and noise margin), noise immunity is more practical for CMOS devices because CMOS outputs are normally within 50mV of supply rails.

Noise immunity increases as the input pulse width becomes less than the propagation delay of the circuit. This condition is often described as AC noise immunity. Further information on noise immunity is given in Application Note AN6587, "Noise Immunity of B-series CMOS Integrated Circuits". See Section 8, "How to Use AnswerFAX", in this selection guide.

Clock Rise and Fall Time Requirements

Most CMOS clocked devices have maximum rise and fall time ratings (normally 5ms to 15ms). With longer rise or fall times, a device may not function properly because of data ripple through, false triggering problems, etc. Some B-series CMOS counters have Schmitt-trigger shaping circuits built into the clock circuit, removing the restriction for input rise or fall times. Long rise and fall times on CMOS buffer-type inputs cause increased power dissipation which may exceed device capability for operating power supply voltages greater than 5V.

Parallel Clocking

Process variations leading to differences in input threshold voltage among random device samples can cause loss of data between certain synchronously clock sequential circuits, as shown in Figure 6. This problem can be avoided if the maximum clock rise time $(t_{\text{R}}C_{\text{L}})$ for cascading any two CMOS sequential devices is limited in accordance with the following equation:

B-Series Types

$$Maximum t_R C_L = \frac{0.8V_{DD}(V)}{1.15V} \times t_P(ns)$$

where $t_P = t_{PHL}$ or t_{PLH} (whichever is smaller) for the unit A in Figure 6 as specified on the device data sheet at the specified value of V_{DD} and loading conditions. Schmitt-trigger circuits such as the CD4093B are an ideal solution to applications requiring wave-shipping.

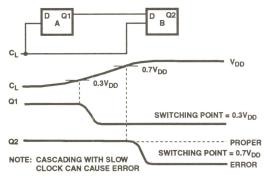


FIGURE 6. ERROR EFFECT THAT RESULTS FROM A SLOW CLOCK IN CASCADED CIRCUITS

Three-State Logic

Three-state logic can be easily implemented by use of a transmission gate in the output circuit; this technique provides a solution to the wire-OR problem in many cases.

Chip Assembly and Storage

Harris CMOS integrated circuits are provided in a chip from (H suffix) to allow customer design of special and complex circuits to suit individual needs. CMOS chips are electrically identical to and offer the features of their counterparts sealed in ceramic and plastic packages. The following paragraphs describe mounting considerations, packaging, shipping and storage criteria, handling criteria, visual inspection criteria, testing criteria, and bonding pad layout and dimensions for each chip.

Mounting Considerations

All CMOS chips are non-gold backed and require the use of epoxy mounting, conductive silver paste or equivalent is recommended. In any case the manufacturer's recommendations for storage and use should be followed.

In CMOS circuits MOS-transistor P-channel substrates (N-type bulk material) are connected to $V_{\rm DD}$, therefore, when chips are mounted and a conductive paste is used, care must be taken to keep the active substrate isolated from ground or other circuit elements.

Packing, Shipping, and Storage Criteria

Solid-state chips, being small in size and unencapsulated, are physically fragile and require special handling consideration as follows:

- Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
 - Storage Temperature, 40°C Max
 - Relative Humidity, 50% Max
 - Clean, Dust-Free Environment
- The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
- During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
- After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to a moist and contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably affect their performance and/or reliability.

Handling Criteria

The user should find the following suggested precautions helpful in handling CMOS chips.

Because of the extremely small size and fragile nature of chips, the equipment designer should exercise care in handling these devices.

For additional handling considerations for CMOS devices, refer to Application Note AN6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits". See Section 8, "How to Use AnswerFAX". in this selection guide.

- Grounding
 - Bonders, pellet pick-up tools, table tops, trim and form tools, sealing equipment, and other equipment used in chip handling should be properly grounded.
 - The operator should be properly grounded.
- · In-Process Handling
 - Assemblies or subassemblies of chips should be transported and stored in conductive carriers.
 - All external leads of the assemblies or subassemblies should be shorted together.
- · Bonding Sequence
 - Connect V_{DD} first to external connections, for example, terminal 14 of the CD4001BH.
 - Remaining functions may be connected to their external connections in any sequence.
- Testing
 - Transport all assemblies of chips in conductive carriers.
 - In testing chip assemblies or subassemblies, the operator should be properly grounded.

Visual Inspection Criteria

All standard commercial CMOS chips undergo a visual inspection which is patterned after MIL-STD-883, Method 2010, Condition B with modifications reflecting CMOS requirements.

Testing Criteria

CMOS chips are DC electrically tested 100% in accordance with the same standards prescribed for Harris devices in standard packages.

Device Testing

Harris CMOS circuits are 100% tested by circuit probe in the wafer stage and are 100% tested again after they have been packaged. DC tests of Harris devices are performed at 5V, 10V, 15V, and 20V; functionality is checked at 2.8V, 17V, and 20V. Sample testing is used to assure adherence to quality requirements and AC specifications.

Static test, high speed functional and DC parametric tests, are performed at wafer and package stages by means of a Teradyne 325 test set or equivalent.

Users should follow the sequences below when testing CMOS devices:

- 1. Insert the device into the test socket.
- 2. Apply V_{DD}.
- 3. Apply the input signal.
- 4. Perform the test.
- 5. On completion of test, remove the input signal.

- 6. Turn off the power supply (VDD).
- Remove the device from the test socket and insert it into a conductive carrier. CMOS devices under test must not be exposed to electrostatic discharge or forward biasing of the intrinsic protective diodes shown in Figure 3.

Detailed information on the techniques employed in the testing of Harris CMOS integrated circuits are described in Application Note AN6532, "Fundamentals of Testing CMOS Integrated Circuits". See Section 8, "How to Use Answer-FAX", in this selection guide.

Device Mounting

Integrated circuits are normally supplied with lead-tin plated leads to facilitate soldering into circuit boards. In those relatively few applications requiring welding of the device leads, rather than soldering, the devices may be obtained with nickel-plated Kovar leads (See MIL-I-38535). It should be recognized that this type of plating will not provide complete protection against lead corrosion in the presence of high humidity and mechanical stress.

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead. It is also extremely important that the ends of bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

High Voltage B-Series CMOS Integrated Circuits

Harris CD4000B series types have a maximum DC supply voltage rating of -0.5V to 20V, and a recommended operating supply voltage range of 3V to 18V. The major features of this series are as follows:

- High Voltage (20V) Ratings
- 100% Tested for Quiescent Current at 20V
- 5V. 10V. and 15V Parametric Ratings
- · Standardized, Symmetrical Output Characteristics
- Maximum Input Current of 1µA at 18V Over Full Package Temperature Range; 100nA at 18V and 25°C
- Noise Margin (Full Package Temperature Range) = 1V at V_{DD} = 5V 2V at V_{DD} = 10V 2.5 V at V_{DD} = 15V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of B-Series CMOS Devices".

JEDEC Minimum Standard

Under the sponsorship of the Joint Electron Devices Engineering Council (JEDEC) of the Electronic Industries Association (EIA), minimum industrial standards have been established for the maximum ratings, DC and AC electrical

characteristics of B-series CMOS integrated circuits. The JEDEC standard (JEDEC Tentative Standard No. 13B) defines B-series CMOS integrated circuits as a uniform family of both buffered and unbuffered types that have an absolute DC supply voltage rating of at least 18V.

Buffered CMOS Devices

These are types in which the output "on" impedance is independent of any and all valid input logic conditions, both preceding and present. All such CMOS products are designated by suffix "B" following the basic type number.

Unbuffered CMOS Devices

These are types that meet all B-series specifications except that the logical outputs are not buffered and the noise-immunity voltages, $\rm V_{IL}$ and $\rm V_{IH}$, are specified as 20% and 80%, respectively, of $\rm V_{DD}$ for operation from 5V, 10V, and 17V and 83%, respectively, of $\rm V_{DD}$ for operation from 15V. All such CMOS product are designated by the suffix "UB".

The JEDEC minimum standard also includes in the B-series, CMOS types that have analog inputs or outputs and in addition, have maximum ratings and logical input and output parameters that conform to B-series specifications wherever applicable. These CMOS devices are also designated by the suffix "B".

All B-series CMOS devices can directly replace their A-series counterparts in most applications. The UB types are high voltage versions of corresponding A-series (unbuffered) types.

Commercial A-series types have been obsoleted and replaced by B-series counterparts with only a few exceptions such as the continuing CD4059A types.

The Absolute Maximum Rating - JEDEC table lists the minimum standards established for the maximum ratings and recommended operating conditions for B-series CMOS integrated circuits.

The DC Electrical Specification - JEDEC table shows the JEDEC standards for the DC electrical specifications of CMOS B-series integrated circuits.

Standardized Ratings and Static Characteristics

Harris B-series CMOS integrated circuits meet or exceed the most stringent requirements of the JEDEC B-series specifications. The Absolute Maximum Ratings table shows the standardized maximum ratings and recommended operating supply voltage range for Harris B-series CMOS integrated circuits. The standardized DC electrical specifications for these devices are shown in the DC Electrical Specification table. As with the JEDEC specifications, the Harris standardized characteristics classify the B-series devices into three leakage (quiescent device current) categories. Table 1 lists the Harris types in each category and indicates types that, although they are still B-series types, differ in one or more static characteristics.

The Absolute Maximum Ratings table and the DC Electrical Specification table show that in a number on important respects, Harris has established new performance standards for B-series CMOS logic circuits.

· Tight Limits For All Packages

Harris devices used the same set of limits for all package styles. The JEDEC standard establishes two sets of limits for most DC parameters; a tight set for products having a full operating temperature range of -55°C to +125°C (all Harris devices), and a relaxed set for products having a limited temperature range of -40°C to +85°C. Because Harris supplies only one premium grade of B-series product in all package styles (i.e., fall-out chips are not used), all B-series CMOS devices are specified to the tight set of limits only.

· Improved Voltage Rating

All Harris B-series devices are tested to voltages that insure safe operation at the absolute maximum DC supply voltage rating of 20V. This higher rating permits greater derating for reliable 15V operation, permits greater 15V supply tolerance and peak transients, and permits system use to 18V with confidence.

· Wider Operating Range

All Harris B-series devices have a recommended maximum operating voltage of 18V. The higher limit permits 18V system supply operation, and also permits wider power source tolerance and transients for supplies normally set up to 18V

· Lower Leakage Current

The JEDEC standard establishes three sets of limits for quiescent device current (I_{DD}) intended to match chip complexity to device leakage current as realistically as possible.

For all three levels of chip complexity, all Harris B-series devices (regardless of package) conform to the tighter set of limits established in the standard. In addition, a maximum rating is specified at 20V, as well as at 5V, 10V, and 15V. As a result:

- In current limited applications, CMOS users can depend on one tight leakage limit independent of package style selected.
- Customer use of CMOS product up through 18V is protected by a published tight leakage current specification at 20V (as well as by an input leakage specification at 18V).

Symmetrical Output

Most Harris B-series devices have balanced complementary output drive (i.e., the output high current I_{OH} rating is the same as the output low current I_{OH} rating specified to the tighter set of limits established in the JEDEC standard. The balanced output provides uniform rise and fall time performance, improved system noise energy (dynamic) immunity, optimum device speed for both output switching low-to-high (t_{PLH}) and output switching high-to-low (t_{PHL}), and in general the identical high and low DC and AC characteristics normally associated with a good complementary output drive circuit. MOS system design, simulation, and performance are significantly enhanced by equal high and low DC and AC performance ratings and one tight specification limit for all package styles.

Improved Input Current (Leakage) Ratings

All Harris B-series devices (regardless of package) have a maximum input leakage current (l_{IN}) rating of 100nA specified at voltages up to 18V, and a maximum limit of 1 μA at the upper limit of the package temperature range. Actually, the 100nA rating is a practical specification limited by the inability of commercial test equipment to measure lower currents. Laboratory tests show that input leakage currents of Harris B-series CMOS devices are significantly lower than this limit, typically ranging from 10pA to 100pA.

· Buffered and Unbuffered Gates

The new industry standard establishes a suffix "UB" for CMOS products that meet all B-series specifications except that the logical outputs of the devices are not buffered and the $V_{\rm IL}$ and $V_{\rm IH}$ specifications are relaxed. The suffix "B" defines only buffered output devices in which the output "on" impedance is independent of any and all valid input logic conditions, both preceding and present.

Harris supplies both buffered "B" and unbuffered "UB" versions of a few popular NOR and NAND gates to make available to designers the advantages of both. The following table briefly compares the features of the two versions, a more detailed coverage of the special features of B- and UB- series CMOS gates is provided by Application Note AN6558, "Understanding Buffered and Unbuffered CMOS Characteristics". See Section 8, "How to Use AnswerFAX", in this selection guide.

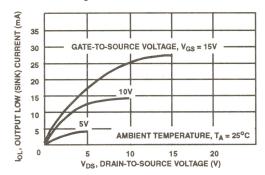


FIGURE 7. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

COMPARISON OF "B" AND "UB"

CHARACTERISTIC	BUFFERED VERSION "B"	UNBUFFERED VERSION "UB"
Propagation Delay (Speed)	Moderate	Fast
Noise Immunity/Margin	Excellent	Good
Output Impedance and Output Transition Time	Constant	Variable
AC Gain	High	Medium
Output Oscillation for Slow inputs	Yes	No
Input Capacitance	Low	High

Reliability

Harris B-series CMOS integrated circuits incorporate the latest improvements in processing technology and plastic and ceramic packaging techniques. Product quality is real time controlled using accelerated temperature group quality screening in which measured DC parameters are criticized against tight B-series limits.

Figure 7 through Figure 10 show the standardized N- and P-channel drain characteristics for B-series CMOS devices, and Figure 11 through Figure 14 show the normalized variation of output source and sink currents with respect to temperature and voltage in these devices.

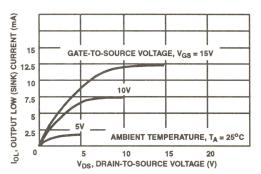


FIGURE 8. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

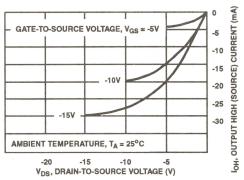


FIGURE 9. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

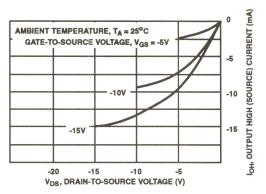


FIGURE 10. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

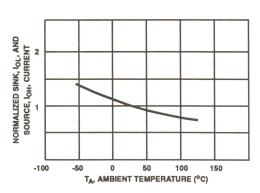


FIGURE 11. VARIATION OF NORMALIZED OUTPUT LOW (SINK)
CURRENT I_{OL} AND OUTPUT HIGH (SOURCE)
CURRENT I_{OH} WITH TEMPERATURE

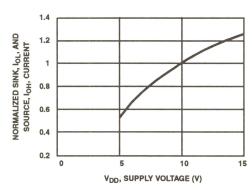


FIGURE 12. VARIATION OF NORMALIZED OUTPUT LOW (SINK)

CURRENT IOL AND OUTPUT HIGH (SOURCE)

CURRENT IOH WITH SUPPLY VOLTAGE

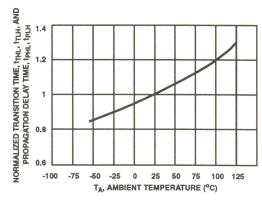


FIGURE 13. VARIATION OF LOW-TO-HIGH (t_{TLH}) AND HIGH-TO-LOW (t_{THL}) TRANSITION TIME, AND LOW-TO-HIGH (t_{PHL}) PROPAGATION DELAY TIME WITH TEMPERATURE

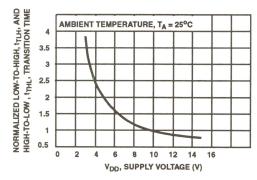


FIGURE 14. VARIATION OF LOW-TO-HIGH ($\mathfrak{t}_{\text{TLH}}$) AND HIGH-TO-LOW ($\mathfrak{t}_{\text{THI}}$) TRANSITION TIME WITH SUPPLY VOLTAGE

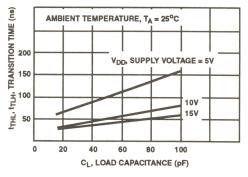


FIGURE 15. VARIATION OF TRANSITION TIME (t_{THL}, t_{TLH}) WITH LOAD CAPACITANCE

B-Series AC Electrical Specifications

B-series AC electrical specifications for individual types are under the following conditions: $V_{DD}=5V$, 10V, and 15V; $T_A=+25^{\circ}C$; $C_L=50pF$; $R_L=200k\Omega$; t_R and $t_F=20ns$. Figure 13 shows the variation of B-series AC parameter with temperature. Figure 14 shows the variation of output transition time with supply voltage. Figure 17 shows the variation of the standardized output transition time with load capacitance.

Maximum propagation delay or transition times for values of C_L other than the specified 50pF can be determined by use of the multiplication factor (usually 2) between the typical and maximum values given in the AC specifications chart included in the technical data for each device applied to the typical curves, and also shown in the device technical data.

B-Series AC Switching Specifications

The AC Electrical Specification table defines the major CMOS AC specifications, with reference to the waveforms shown in Figure 16 through Figure 19. Test conditions of V_{DD} , low capacitance (C_L), and input conditions are given for individual types in the published data.

CMOS Special Products

Harris supplies some special CMOS products that have operating supply voltage ranges and other characteristics that differ from the standardized data specified for B-series CMOS integrated circuits.

These special application types include: interface circuits for level shifting applications to interface CMOS logic levels with different logic types; display drivers non-multiplexed, 4 digit, 7 segment LCD types containing all the circuitry necessary for driving conventional LCD displays without the need for external components, and a video sync generator function.

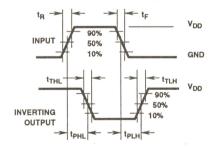
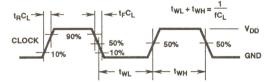


FIGURE 16. TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC



NOTE: Outputs should be switching from 10% V_{DD} to 90% V_{DD} in accordance with the device truth table.

FIGURE 17. CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

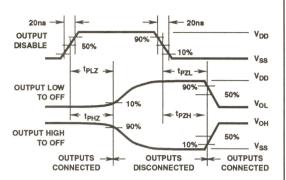


FIGURE 18A.

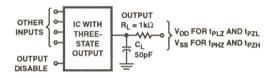
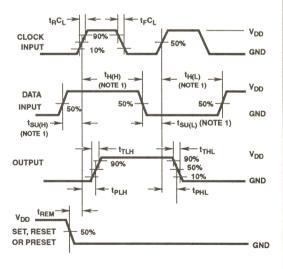


FIGURE 18B.

FIGURE 18. THREE-STATE PROPAGATION DELAY WAVE SHAPES AND TEST CIRCUIT



NOTE:

1. (H) or (L) Optional

FIGURE 19. SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

Absolute Maximum Ratings JEDEC Standard for DC Specifications of B-Series CMOS Integrated Circuits (Note 1 and Note 2)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

DC Electrical Specification JEDEC Standard for DC Specifications of B-Series CMOS Integrated Circuits

		TEST	т		(NOT	re 3)		+25°C		(NOTE 4) T _{HIGH}		
PARAMETERS	SYMBOL	CONDITIONS	RANGE	(V)	MIN	MAX	MIN	TYP	MAX	MIN	MAX	UNIT
Quiescent	I _{DD}	$V_{IN} = V_{SS}$ or V_{DD}	Mil	5	-	0.25	-	-	0.25	-	7.5	μА
Device Current		All Valid Input Combinations		10	-	0.5	-	-	0.5	-	15	μА
Gates			-	15	-	1	-	-	1	-	30	μА
			Comm	5	-	1	-	-	1		7.5	μА
				10	-	2	-	-	2		15	μА
				15	-	4	-	-	4	-	30	μА
Buffers,	I _{DD}	V _{IN} = V _{SS} or V _{DD}	Mil	5	-	1	-	-	1	-	30	μА
Flip-Flops		All Valid Input Combinations		10		2	-	-	2	-	60	μА
				15	-	4	-	-	4	-	120	μА
			Comm	5	-	4	-	- ,	4	-	30	μА
				10	-	8	-	-	8	-	60	μА
				15	-	16	-	-	16	-	120	μА
MSI	I _{DD}	V _{IN} = V _{SS} or V _{DD} All Valid Input Combinations	Mil	5	-	5	-	-	5	-	150	μА
				10	-	10	-	-	10	-	300	μА
				15	-	20	-	-	20	- 600	600	μА
			Comm	5	-	20	-	-	20	-	150	μА
				10	-	40	-	-	40	-	300	μА
				15	-	80	-	-	80		600	μА
Low Level	V _{OL}	$V_{IN} = V_{SS}$ or V_{DD} $ I_{O} < 1\mu A$	All	5	-	0.05	-	-	0.05	-	0.05	٧
Output Voltage		11 ₀ 1 < 1µA		10	-	0.05	-	-	0.05	-	0.05	٧
				15	-	0.05	-	-	0.05	-	0.05	٧
High Level	V _{OH}	$V_{IN} = V_{SS}$ or V_{DD} $ I_{O} < 1\mu A$	All	5	4.95	-	4.95	-	-	4.95	-	٧
Output Voltage		1101 < 1μΑ		10	9.95	-	9.95	-	-	9.95	-	٧
				15	14.95	-	14.95	-	-	14.95	-	٧

For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX. See Section 8, "How to use AnswerFAX", in this selection guide.

DC Electrical Specification JEDEC Standard for DC Specifications of B-Series CMOS Integrated Circuits (Continued)

		TEST	TEMP.	V _{DD}	(NOT	re 3)		+25°C		(NOTE 4) T _{HIGH}		×
PARAMETERS	SYMBOL	CONDITIONS	RANGE	(V)	MIN	MAX	MIN	TYP	MAX	MIN	MAX	UNIT
Input Low Voltage	V _{IL}	$V_0 = 0.5V \text{ or } 4.5V$	All	5	-	1.5	-	-	1.5	-	1.5	٧
B Types		$V_O = 1V \text{ or } 9V$ $V_O = 1.5V \text{ or } 13.5V$		10	-	3	-	-	3	-	3	٧
		ll _O l <1μΑ		15		4	-	-	4	1.	4	٧
UB Types				5	-	1	-	-	1	-	1	٧
				10	-	2	-	-	2	-	2	٧
				15	-	2.5	-	-	2.5	-	2.5	٧
Input High Voltage	V _{IH}	$V_0 = 0.5V \text{ or } 4.5V$	All	5	3.5	-	3.5	-	-,	3.5	-	٧
B Types		$V_O = 1V \text{ or } 9V$ $V_O = 1.5V \text{ or } 13.5V$		10	7	-	7	-	-	7	-	٧
		II _O I <1μΑ		15	11	-	- 11 -	-	11	-	٧	
UB Types			5	4	-	4	-	-	4	-	٧	
				10	8	-	8	-	-	8	-	٧
				15	12.5	-	12.5	-		12.5	-	٧
Output Low (Sink)	l _{OL}	$V_0 = 0.4V$	Mil	5	0.64	-	0.51	-	-	0.36	-	mA
Current		$V_{IN} = 0V \text{ or } 5V$ $V_{O} = 0.5V$		10	1.6	-	1.3	0	0.9	-	mA	
		V _{IN} = 0V or 10V V _O = 1.5V		15	4.2	-	3.4	-		2.4	-	mA
		V _{IN} = 0V or 15V	Comm	5	0.52	-	0.44	-	-	0.36	-	mA
				10	1.3	-	1.1	-	-	0.9	-	mA
				15	3.6	-	3.0	-	-	2.4	-	mA
Output High	I _{OH}	V _O = 4.6V	Mil	5	-0.25	-	-0.2	-	-	-0.14	-	mA
(Source) Current		$V_{IN} = 0V \text{ or } 5V$ $V_{O} = 9.5V$		10	-0.62	-	-0.5	-	-	-0.35	-	mA
		V _{IN} = 0V or 10V V _O = 13.5V		15	-1.8	-	-1.5	-	-	-1.1	-	mA
		V _{IN} = 0V or 15V	Comm	5	-0.2	-	-0.16	-	-	-0.12	-	mA
				10	-0.5	-	-0.4	-	-	-0.3	-	mA
				15	-1.4	-	-1.2	-	-	-1.0	-	mA
Input Current	I _{IN}	V _{IN} = 0V or 15V	Mil	15	-	±0.1	-	-	±0.1	-	±1	μА
		V _{IN} = 0V or 15V	Comm	15	-	±0.3	-	-	±0.3	-	±1	μА
Three-State	I _{OUT} Max	V _{IN} = 0V or 15V	Mil	15	-	±0.4	-	-	±0.4	-	±12	μА
Output Leakage Current		V _{IN} = 0V or 15V	Comm	15	-	±1.6	-	-	±1.6	-	±12	μА
Input Capacitance Per Unit Load	C _{IN}	Any Input	All	-		-		-	7.5	-	-	pF

NOTES:

- 1. Voltages referenced to V_{SS}.
- 2. Reprinted from JEDEC Standard No. 13-B, "JEDEC Standard Specification for Description of B-Series CMOS Devices".
- 3. T_{LOW} = -55°C for Military Temperature Range Device, -40°C for Commercial Temperature Device (All Harris Devices).
- 4. $T_{HIGH} = +125^{\circ}C$ for Military Temperature Range Device, $+85^{\circ}C$ for Commercial Temperature Range Device.

[‡] For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX. See Section 8, "How to use AnswerFAX", in this selection guide.

Standardized Absolute Maximum Ratings For B-Series CMOS Integrated Circuits

Tallian and the state of the st	ower megrates onesite
DC Supply Voltage, V _{DD}	Power Dissipation Per, P _D
Voltage Reference to V _{SS} Terminal0.5V to +20V	$T_A = -55^{\circ}C \text{ to } +100^{\circ}C \dots 500 \text{mW}$
Input Voltage, All Inputs0.5V to V _{DD} +0.5V	$T_A = +100$ °C to $+125$ °C Derate Linearly at 12 mW/°C to 200 mW
DC Input Current,	Device Dissipation Per Output Transistor
For Any One Input	For T _A = Full Package Temperature Range
Lead Temperature (During Soldering)	(All Package Test)
At Distance 1/16in. ± 1/32in. (1.59mm ± 0.79mm)	Operating Temperature Range, T _A 55°C to +125°C
from Case for 10s Max	Storage Temperature, T _{STG} 65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Supply, Voltage Range

For T_A = Full Package Temperature Range. +3V to +18V

Standardized DC Electrical Specification For B-Series CMOS Integrated Circuits

		TEST	CONDITI	ONS		LI	MITS			+25°C		
PARAMETERS	SYMBOL	V _o (V)	V _{IN} (V)	V _{DD} (V)	-55°C	-40°C	+85°C	+125°C	MIN	TYP	MAX	UNIT
Quiescent Device Current	I _{DD} Max	-	0, 5	5	0.25	0.25	7.5	7.5	-	0.01	0.25	μА
Current		-	0, 10	10	0.5	0.5	15	15	-	0.01	0.5	μА
Gates, Inverters (Note 1)		-	0, 15	15	1	1	30	30	-	0.01	1	μА
(Note 1)		, -	0, 20	20	5	5	150	150	-	0.02	5	μА
Buffers, Flip- Flops, Latches,		-	0, 5	5	1	1	30	30	-	0.02	1	μА
Multi-Level Gates (MSI-1 Types)		-	0, 10	10	2	2	60	60	-	0.02	2	μА
(Note 1)		-	0, 15	15	4	4	120	120	-	0.02	4	μА
		-	0, 20	20	20	20	600	600	-	0.04	20	μА
Complex Logic (MSI-2 Types)		-	0, 5	5	5	5	150	150	-	0.04	5	μА
(Note 1)		-	0, 10	10	10	10	300	300	-	0.04	10	μА
		-	0, 15	15	20	20	600	600	-	0.04	20	μА
		-	0, 20	20	100	100	3000	3000	-	0.08	100	μА
Output Low (Sink) Current Min	I _{OL} Min	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
Current Will		0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	mA
		1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8	-	mA
Output High (Source) Current, Min	I _{OH} Min	4.6	0, 5	5	-6.4	-0.61	-0.42	-0.36	-0.51	-1	-	mA
Ourietti, iviitt		2.5	0, 5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	٠.	mA
		9.5	0, 10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	mA
		13.5	0, 15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	mA

For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX. See Section 8, "How to use AnswerFAX", in this selection guide.

5-14

Standardized DC Electrical Specification For B-Series CMOS Integrated Circuits (Continued)

		TEST	CONDITI	ONS		LI	MITS			+25°C		
PARAMETERS	SYMBOL	V _o (V)	V _{IN} (V)	V _{DD} (V)	-55°C	-40°C	+85°C	+125°C	MIN	TYP	MAX	UNIT
Output Voltage Low- Level	V _{OL} Max	-	0, 5	5	0.05		-	0	0.05	٧		
Level		-	0, 10	10	0.05			-	0	0.05	٧	
			0, 15	15		().05		-	0	0.05	٧
Output Voltage	V _{OH} Min	-	0, 5	5		4	1.95		4.95	5	-	٧
High-Level		-	0, 10	10		9	9.95		9.95	10	-	٧
			0, 15	15		1	4.95		14.95	15	-	٧
Input Low Voltage	V _{IL} Max	0.5, 4.5	-	5			1.5		-	-	1.5	٧
		1, 9	-	10	3		-	-	3	٧		
B Types		1.5, 13.5		15			4		-	-	4	٧
UB Types		0.5, 4.5	-	5	1		-	-	1	٧		
		1, 9	-	10	2			-	-	2	٧	
		1.5, 13.5	-	15			2.5		-	-	2.5	٧
Input High Voltage	V _{IH} Max	0.5, 4.5	-	5			3.5		3.5	-	-	٧
		1, 9	-	10			7		7	-	-	٧
B Types		1.5, 13.5	-	15			11		11	-	-	٧
UB Types		0.5, 4.5	-	5			4		4	-	-	٧
		1, 9	-	10			8		8	-	-	٧
		1.5, 13.5	-	15	12.5			12.5	-	-	٧	
Input Current	I _{IN} Max	-	0, 18	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	μА
Three-State Output Leakage Current	I _{OUT} Max	0, 18	0, 18	18	±0.4	±0.4	±12	±12	-	±10 ⁻⁴	±0.4	μА

NOTE:

^{1.} Classifications of Harris CMOS B-Series Types are Shown in Table 1.

For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX.
 See Section 8, "How to use AnswerFAX", in this selection guide.

AC Electrical Specifications Definitions

PARAMETERS	SYMBOL	MIN	MAX	NOTES
PROPAGATION DELAY				
Outputs Going High to Low	t _{PHL}	-	Х	-
Outputs Going Low to High	t _{PLH}	-	Х	-
OUTPUT TRANSITION TIME	-			
Outputs Going High to Low	t _{THL}	-	Х	-
Outputs Going Low to High	t _{TLH}	-	Х	
PULSE WIDTH		9		
Set, Reset, Preset, Enable, Disable, Strobe, Clock	t _{WL} or t _{WH}	×	-	1
Clock Input Frequency	f _{CL}	-	Х	1, 2
Clock Input Rise and Fall Time	t _{RCL} , t _{FCL}	-	х	-
Set-Up Time	t _{su}	X	-	1
Hold Time	t _H	X	-	1
Removal Time - Set, Reset, Preset-Enable	t _{REM}	х		1
THREE-STATE DISABLE DELAY TIMES		•	•	•
High Level to High Impedance	t _{PHZ}	-	х	-
High Impedance to Low Level	t _{PZL}	-	Х	-
Low Level to High Impedance	t _{PLZ}	-	Х	-
High Impedance to High Level	t _{PZH}	-	Х	-

NOTES:

- 1. By placing a defining Min or Max in front of definition, the limits can change from Min to Max, or vice versa.
- 2. Clock input waveform should have a 50% duty cycle and be such as to cause the Outputs to be switching from 10% V_{DD} to 90% V_{DD} in accordance with the device truth table.

TABLE 1. CLASSIFICATION OF HARRIS B-SERIES CMOS INTEGRATED CIRCUITS ACCORDING TO CIRCUIT COMPLEXITY

GATES/IN	VERTERS	LATCHES/M	FLIP-FLOP/ IULTI-LEVEL 5 (MSI-1)	COMPLEX LOGIC (MSI-2)			
CD4001B	CD4069UB	CD4009UB (Note 1)	C04093B	CD4006B	CD4055B (Note 1)	CD4532B	
CD4001UB	CD4070B	CD4010B (Note 1)	CD4095B	CD4008B	CD4056B (Note 1)	CD4536B	
CD4002B	CD4071B	CD4013B	CD4096B	CD4014B	CD4060B	CD4541B	
CD4007UB	CD4072B	CD4019B	CD4098B	CD4015B	CD4063B	CD4543B	
CD4011B	CD4073B	CD4027B	CD4502B (Note 1)	CD4017B	CD4067B (Note 1)	CD4555B	
CD4011UB	CD4075B	CD4030B	CD4503B	CD4018B	CD4076B	CD4556B	

For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX.
 See Section 8, "How to use AnswerFAX", in this selection guide.
 5-16

TABLE 1. CLASSIFICATION OF HARRIS B-SERIES CMOS INTEGRATED CIRCUITS ACCORDING TO CIRCUIT COMPLEXITY (Continued)

GATES/II	NVERTERS	LATCHES/N	FLIP-FLOP/ IULTI-LEVEL 5 (MSI-1)	со	MPLEX LOGIC (MS	SI-2)
CD4012B	CD4077B	CD4041UB (Note 1)	CD4504B	CD4020B	CD4089B	CD4560B
CD4016B (Note 1)	CD4078B	CD4042B	CD4519B	CD4021B	CD4094B	CD4566B
CD4023B	CD4081B	CD4043B	CD40106B	CD4022B	CD4097B (Note 1)	CD4585B
CD4025B	CD4082B	CD4044B	CD40107B (Note 1)	CD4024B	CD4099B	CD4724B
CD4048B	CD40117B	CD4047B	CD40109B (Note 1)	CD4026B	CD4508B	CD14538B
CD4066B (Note 1)	CD4572UB	CD4049UB (Note 1)	CD40174B	CD4028B	CD4510B	CD40100B
CD4068B		CD4050B (Note 1)	CD40175B	CD4029B	CD4511B (Note 1)	CD40102B
		CD4085B	CD40257B	CD4031B	CD4512B	CD40103B
		CD4086B		CD4033B	CD4514B	CD40105B
				CD4034B	CD4515B	CD40110B (Note 1)
				CD4035B	CD4516B	CD40147B
				CD4040B	CD4517B	CD40160B
				CD4045B (Note 1)	CD4518B	CD40161B
				CD4046B (Note 1)	CD4520B	CD40163B
				CD4051B (Note 1)	CD4521B	CD40192B
				CD4052B (Note 1)	CD4522B	CD40193B
				CD4053B (Note 1)	CD4527B	CD40194B
				CD4054B (Note 1)	CD4529B	

NOTE:

^{1.} Indicates types for which, because of special design requirements, one or more static characteristics differ from the standardized data. Refer to data pages on these types for specific differences.

Enhanced Product

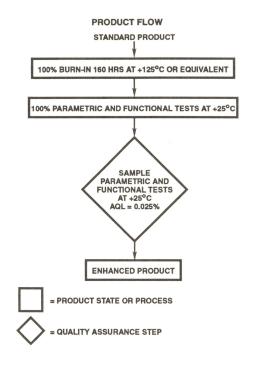
STANDARD IC CIRCUITS

		SUFFIX "X"		
Burn-In Time (Note	1)	160 Hours		
Temperature (Note	+125°C			
Bias Voltage	CD4000B	15V		
	Special	Differs by Type		

PRODUCT IDENT	IFICATION				
All Enhanced Product is Identified by a Suffix "X"					
Examples: Standard CD4001BE	Enhanced CD4001BEX				

NOTE:

 Or equivalent means equivalent time-temperature /voltage resulting in the same activation energy.



CMOS LOGIC ICs

6

PRODUCT SELECTION GUIDE

HARRIS MILITARY GRADE/HIGH-RELIABILITY PRODUCTS

	PAGE
MILITARY GRADE/HIGH-RELIABILITY PRODUCTS	6-3
Introduction	6-3
JAN (Joint Army Navy)	6-3
SMD (Standard Military Drawing)	6-3
Harris Class B Compliant	6-3
Harris Class B "Equivalent"	6-3
Non-Standard Product Offerings	6-3
HIGH SPEED CMOS LOGIC ICS - HC/HCT SERIES	6-4
Guide to the Reliability Class and Package of Harris High-Reliability CD54HC/HCT ICs	6-4
Data Sheet AnswerFAX Document Listing	6-4
Guide to SMD and DESC Part Numbers	6-8
Harris SMD and DESC Parts List, Digital - Logic CD54HC/HCT	6-8
Lot Screening Tests	6-12
Product Flow Diagram	6-13
Transistor Count Per Device	6-13
Absolute Maximum Ratings	6-15
Standard DC Electrical Specifications - CD54HC Series	6-15
Standard DC Electrical Specifications - CD54HCT Series	6-16
Table 1. Standard TTL Output Load Characteristics - CD54HC/HCT Series.	6-17
ADVANCED CMOS LOGIC ICS - AC/ACT SERIES‡	6-18
Guide to the Reliability Class and Package of Harris High-Reliability CD54AC/ACT ICs	6-18
Data Sheet AnswerFAX Document Listing	6-18
Lot Screening Tests	6-19
Product Flow Diagram	6-20
Transistor Count Per Device	6-20
Absolute Maximum Ratings	6-21
Standard DC Electrical Specifications - CD54AC Series	6-21
Standard DC Electrical Specifications - CD54ACT Series	6-22
Prerequisite for Switching - AC/ACT.	6-22

For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX.
 See Section 8, "How to use AnswerFAX", in this selection guide.

Harris Military Grade/High-Reliability Products (Continued)

		PAGE
CI	MOS LOGIC ICs - CD4000B SERIES.	6-23
	Features	6-23
	Buffered vs Unbuffered Gates	6-23
	Compliance to MIL-STD-883	6-23
	JAN M38510 CMOS ICs	6-23
	Product Ordering Information.	6-24
	Description of Data Supplied	6-25
	JAN or Class B Product	6-25
	Suffix 3A Harris /883 Full Compliant	6-25
	Suffix 3 Harris /883 Non Compliant	6-25
	Product Number Selection Guide	6-26
	MIL-I-38535 to Harris Hi-Rel Types Sorted by JAN Type.	6-34
	SMD or DESC Parts List	6-34
	Lot Screening Tests	6-34
	Total Lot Screening For High-Reliability CD4000B Series ICs.	6-35
	Product Flow Diagrams	6-36
	Absolute Maximum Ratings	6-37
	Device Classification for Leakage Current	6-37
	Classification According To Circuit Complexity	6-37
	DC Electrical Specifications - Standard "B" Series Devices	6-38
	Non-Standard DC Electrical Specifications	6-40
	Non-Standard DC Electrical Specifications "B" Series Devices	6-40
	Switching Characteristics	6-50
	Switching Characteristics at +25°C	6-50
	Gate Count	6-56
	Static Life Test and Burn-In Test Circuit Connections	6-57
Q	UALITY ASSURANCE AND RELIABILITY	6-59
	MIL-STD-883, Notice 5	6-59
	Electrical Test Requirements for Non-JAN Lot Conformance Tests	6-59
	Life Test Reliability Data	6-60
	Activation Energy	6-60
	Temperature Acceleration Factor	6-60
	Reliability Data	6-60

Military Grade/High-Reliability Products

Introduction

Section 6 contains information on the extensive line of CMOS Logic military and aerospace products currently available from Harris Semiconductor. These products are processed and screened in accordance with military, internal and special customer high-reliability specifications to meet the demands of modern military, aerospace, and critical industrial and scientific applications. Harris high-reliability products include a broad complement of products that encompass a wide variety of circuit functions and device types.

This section describes the screening levels to which the types in each product series are supplied and includes product flow charts, detailed screening procedures, and test limits that precisely define each level. In addition, a data sheet AnswerFAX document list is provided for each product series.

Harris High Reliability Products are offered in the following Military grades:

JAN (Joint Army Navy)

Registered trademark of the U.S. Government indicating that a device is fully compliant to MIL-I-38535. The Defense Electronics Supply Center (DESC) maintains a continuing audit of manufacturing compliance. There are two product assurance classes available for MIL-I-38535 products (Class S and B). Devices are defined and identified by their particular detail specification or "slash sheet" number issued by DESC (e.g. JM38510/05754BEA). The IC manufacturers who are qualified to supply products to a particular M38510 slash sheet are identified in the Qualified Products List (QPL) issued by DESC.

SMD (Standard Military Drawing)

The SMD evolved from the DESC drawing program which was viewed as a preliminary specification prior to JAN approval. SMDs were created to control the proliferation of non-standard Source Control Drawings. The Standard Military Drawing provides standardized MIL-STD-833 processing in conjunction with non-JAN devices as specified in paragraph 1.2.1 of MIL-STD-883. These devices are defined and identified by their Standard Military Drawing number issued by DESC (e.g. 5962-8772401EA). The manufacturers qualified to supply a particular SMD device are listed in the back of the individual Standard Military Drawing.

Harris Class B Compliant

These devices are fully compliant to MIL-STD-883, Class B and are identified by the /883 or 3A suffix on the Harris part number. The parametric limits for an /883 and 3A data sheets are controlled by the manufacturer rather than a governmental agency, and therefore, there may be differences in the test methodology and actual limits for "similar" devices made by different manufacturers.

This manufacturer control of the /883 and 3A specifications allows the offering of /883-level products long before they might become available as MIL-I-38535 or SMD devices. In many cases, Harris actually specifies /883 and 3A devices with more stringent conditions than those appearing on the MIL-I-38535 slash sheet or SMD describing the same generic device. Harris recommends using our /883 and 3A data sheets as the baseline for new military or aerospace source control drawings.

Harris Class B "Equivalent"

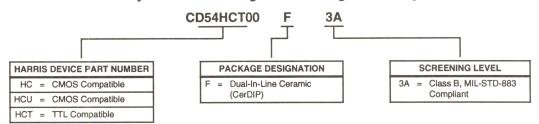
These devices are processed and tested in a manner equivalent to the MIL-STD-883 compliant devices. They may not be classified as compliant since government standards have not been established for processing these types of components (e.g. Ram Modules). The Class B "Equivalent" products can be identified by the -8, /B, or /3 suffix on the Harris part number.

Non-Standard Product Offerings

Harris understands the need for customer generated Source Control Drawings with non-standard parameter and/or screening requirements. A Customer Engineering Department is responsible for efficiently expediting the SCDs through a comprehensive review process. Our Customer Engineering Group compares the SCD to its closest equivalent product grade and works closely with the Product Engineer, Manufacturing Engineer, Design Engineer, or applicable individual to compare Harris' screening ability against the customer's non-standard requirement(s). For products processed to non-standard requirements, a unique part number suffix is assigned.

Harris shares the military's objective to utilize standards wherever possible. We recommend using our /883 data sheets as guidelines for generating new Source Control Drawings. In instances where an available military specification or Harris /883 data sheet is inappropriate, it is Harris' sincerest wish to work closely with the customer in establishing an acceptable procurement document. For this reason, the customer is requested to contact the nearest Harris Sales Office or Representative before finalizing the Source Control Drawing. Harris looks forward to working with the customer prior to implementation of the formal drawing so that both parties may create a mutually acceptable procurement document.

Guide to the Reliability Class and Package of Harris High-Reliability CD54HC/HCT ICs



Data Sheet AnswerFAX Document Listing

TYPE NUMBER			(NOTE 1) NUMBER		ANSWERFAX
CMOS LOGIC	TTL LOGIC	DESCRIPTION	OF LEADS	CLASSIFICATION	DOCUMENT NUMBER
CD54HC00F3A	CD54HCT00F3A	Quad 2-Input NAND Gate	14	SSI	3753
CD54HC02F3A	CD54HCT02F3A	Quad 2-Input NOR Gate	14	SSI	3754
CD54HC03F3A	CD54HCT03F3A	Quad 2-Input NAND Gate with Open Drain	14	SSI	3755
CD54HC04F3A	CD54HCT04F3A	Hex Inverter	14	SSI	3756
CD54HC08F3A	CD54HCT08F3A	Quad 2-Input AND Gate	14	SSI	3757
CD54HC10F3A	CD54HCT10F3A	Triple 3-Input NAND Gate	14	SSI	3758
CD54HC11F3A	CD54HCT11F3A	Triple 3-Input AND Gate	14	SSI	3759
CD54HC14F3A	CD54HCT14F3A	Hex Inverting Schmitt Trigger	14	SSI	3760
CD54HC20F3A	CD54HCT20F3A	Dual 4-Input NAND Gate	14	SSI	3761
CD54HC21F3A	CD54HCT21F3A	Dual 4-Input AND Gate	14	SSI	3762
CD54HC27F3A	CD54HCT27F3A	Triple 3-Input NOR Gate	14	SSI	3763
CD54HC30F3A	CD54HCT30F3A	8-Input NAND Gate	14	SSI	3764
CD54HC32F3A	CD54HCT32F3A	Quad 2-Input OR Gate	14	SSI	3765
CD54HC42F3A	CD54HCT42F3A	BCD-to-Decimal Decoder (1-to-10)	16	MSI	3766
CD54HC73F3A	-	Dual J-K Flip-Flop with Reset	14	FF	3767
CD54HC74F3A	CD54HCT74F3A	Dual D Flip-Flop with Set and Reset	14	FF	3768
CD54HC75F3A	CD54HCT75F3A	Quad Bistable Transparent Latch	16	FF	3769
CD54HC85F3A	CD54HCT85F3A	4-Bit Magnitude Comparator	16	MSI	3770
CD54HC86F3A	CD54HCT86F3A	Quad 2-Input EXCLUSIVE-OR Gate	14	SSI	3771
CD54HC107F3A	CD54HCT107F3A	Dual J-K Flip-Flop with Reset	14	FF	3772
CD54HC109F3A	CD54HCT109F3A	Dual J-K Flip-Flop with Set and Reset	16	FF	3773
CD54HC112F3A	CD54HCT112F3A	Dual J-K Flip-Flop with Set and Reset	16	FF	3774
CD54HC123F3A	CD54HCT123F3A	Dual Retriggerable Monostable Multivibrator with Reset	16	MSI	3775
CD54HC125F3A	CD54HCT125F3A	Quad Three-State Buffer	14	MSI	3776
CD54HC126F3A	CD54HCT126F3A	Quad Three-State Buffer	14	MSI	3777
CD54HC132F3A	CD54HCT132F3A	Quad 2-Input NAND Schmitt Trigger	14	SSI	3778

Data Sheet AnswerFAX Document Listing (Continued)

TYPE NUMBER			(NOTE 1)		ANSWERFAX	
CMOS LOGIC	TTL LOGIC	DESCRIPTION	OF LEADS	CLASSIFICATION	DOCUMENT NUMBER	
CD54HC138F3A	CD54HCT138F3A	3-to-8-Line Decoder/Demultiplexer, Inverting	16	MSI	3779	
CD54HC139F3A	CD54HCT139F3A	Dual 2-of-4-Line Decoder/Demultiplexer	16	MSI	3780	
CD54HC147F3A	-	10-to-4-Line Priority Encoder	16	MSI	3781	
CD54HC151F3A	CD54HCT151F3A	8-Input Multiplexer	16	MSI	3782	
CD54HC153F3A	CD54HCT153F3A	Dual 4-Input Multiplexer	16	MSI	3783	
CD54HC154F3A	CD54HCT154F3A	4-to-16-Line Decoder/Demultiplexer	24	MSI	3784	
CD54HC157F3A	CD54HCT157F3A	Quad 2-Input Multiplexer	16	MSI	3785	
CD54HC158F3A	CD54HCT158F3A	Quad 2-Input Multiplexer, Inverting	16	MSI	3786	
CD54HC160F3A	CD54HCT160F3A	Synchronous BCD Decade Counter, Asynchronous Reset	16	MSI	3787	
CD54HC161F3A	CD54HCT161F3A	Synchronous 4-Bit Binary Counter, Asynchronous Reset	16	MSI	3788	
CD54HC162F3A	CD54HCT162F3A	Synchronous BCD Decade Counter, Synchronous Reset	16	MSI	3789	
CD54HC163F3A	CD54HCT163F3A	Synchronous 4-Bit Binary Counter, Synchronous Reset	16	MSI	3790	
CD54HC164F3A	CD54HCT164F3A	8-Bit Serial-In/Parallel-Out Shift Register	14	MSI	3791	
CD54HC165F3A	CD54HCT165F3A	8-Bit Parallel-In/Serial-Out Shift Register	16	MSI	3792	
CD54HC166F3A	CD54HCT166F3A	8-Bit Parallel-In/Serial-Out Shift Register	16	MSI	3793	
CD54HC173F3A	CD54HCT173F3A	Quad D-Type Flip-Flop, Three-State	16	MSI	3794	
CD54HC174F3A	CD54HCT174F3A	Hex D-Type Flip-Flop with Reset	16	MSI	3795	
CD54HC175F3A	CD54HCT175F3A	Quad D-Type Flip-Flop with Reset	16	MSI	3796	
CD54HC190F3A	-	Presettable Synchronous BCD Decade Up/Down Counter	16	MSI	3797	
CD54HC191F3A	CD54HCT191F3A	Presettable Synchronous Up/Down Counter	16	MSI	3798	
CD54HC192F3A	-	Synchronous BCD Decade Up/Down Counter	16	MSI	3799	
CD54HC193F3A	CD54HCT193F3A	Synchronous 4-Bit Binary Up/Down Counter	16	MSI	3800	
CD54HC194F3A	CD54HCT194F3A	4-Bit Bidirectional Universal Shift Register	16	MSI	3801	
CD54HC195F3A	-	4-Bit Parallel Access Shift Register	16	MSI	3802	
CD54HC221F3A	-	Dual Monostable Multivibrator with Reset	16	MSI	3803	
CD54HC237F3A	-	3-to-8-Line Decoder/Multiplexer with Address Latches	16	MSI	3804	
CD54HC238F3A	CD54HCT238F3A	3-to-8-Line Decoder/Demultiplexer	16	MSI	3805	
CD54HC240F3A	CD54HCT240F3A	Octal Buffer/Line Driver, Three-State, Inverting	20	MSI	3806	
-	CD54HCT241F3A	Octal Buffer/Line Driver, Three-State	20	MSI	3807	
CD54HC243F3A	CD54HCT243F3A	Quad Bus Transceiver, Three-State	14	MSI	3808	
CD54HC244F3A	CD54HCT244F3A	Octal Buffer/Line Driver, Three-State	20	MSI	3809	
CD54HC245F3A	CD54HCT245F3A	Octal Bus Transceiver, Three-State	20	MSI	3810	

Data Sheet AnswerFAX Document Listing (Continued)

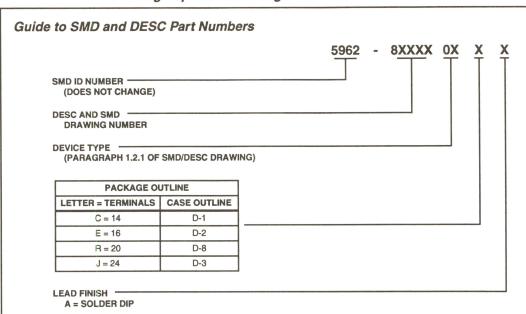
TYPE NUMBER			(NOTE 1) NUMBER OF		ANSWERFAX DOCUMENT	
CMOS LOGIC	TTL LOGIC	DESCRIPTION	LEADS	CLASSIFICATION	NUMBER	
CD54HC251F3A	CD54HCT251F3A	8-Input Multiplexer, Three-State	16	MSI	3811	
CD54HC253F3A		Dual 4-Input Multiplexer, Three-State	16	MSI	3812	
CD54HC257F3A	CD54HCT257F3A	Quad 2-Input Multiplexer, Three-State	16	MSI	3813	
-	CD54HCT258F3A	Quad 2-Line-to-4-Line Data Selector	16	MSI	3814	
CD54HC259F3A	CD54HCT259F3A	8-Bit Addressable Latch	16	MSI	3815	
CD54HC273F3A	CD54HCT273F3A	Octal D-Type Flip-Flop with Reset	20	MSI	3816	
CD54HC280F3A	CD54HCT280F3A	9-Bit Odd/Even Parity Generator/Checker	14	MSI	3817	
CD54HC283F3A	CD54HCT283F3A	4-Bit Full Adder with Fast Carry	16	MSI	3818	
CD54HC297F3A	-	Digital Phase-Locked-Loop	16	MSI	3819	
CD54HC299F3A	CD54HCT299F3A	8-Bit Universal Shift Register, Three-State	20	MSI	3820	
CD54HC354F3A	-	8-Input Multiplexer/Register, Three-State	20	MSI	3821	
CD54HC356F3A	-	8-Input Multiplexer/Register, Three-State	20	MSI	3822	
CD54HC365F3A	CD54HCT365F3A	Hex Buffer/Line Driver, Three-State	16	MSI	3823	
CD54HC366F3A	CD54HCT366F3A	Hex Buffer/Line Driver, Three-State, Inverting	16	MSI	3824	
CD54HC367F3A	CD54HCT367F3A	Hex Buffer/Line Driver, Three-State	16	MSI	3825	
CD54HC368F3A	-	Hex Buffer/Line Driver, Three-State, Inverting	16	MSI	3826	
CD54HC373F3A	CD54HCT373F3A	Octal Transparent Latch, Three-State	20	MSI	3827	
CD54HC374F3A	CD54HCT374F3A	Octal D-Type Flip-Flop, Three-State	20	MSI	3828	
CD54HC377F3A	CD54HCT377F3A	Octal D-Type Flip-Flop with Data Enable	20	MSI	3829	
-	CD54HCT390F3A	Dual Decade Ripple Counter	16	MSI	3830	
CD54HC393F3A	CD54HCT393F3A	Dual 4-Bit Binary Ripple Counter	14	MSI	3831	
-	CD54HCT423F3A	Dual Retriggerable Monostable Multivibrator with Reset	16	MSI	3832	
CD54HC533F3A	CD54HCT533F3A	Octal Transparent Latch, Three-State, Inverting	20	MSI	3833	
CD54HC534F3A	CD54HCT534F3A	Octal D-Type Flip-Flop, Three-State, Inverting	20	MSI	3834	
CD54HC540F3A	-	Octal Buffer/Line Driver, Three-State, Inverting	20	MSI	3835	
CD54HC541F3A	CD54HCT541F3A	Octal Buffer/Line Driver, Three-State	20	MSI	3836	
CD54HC563F3A	-	Octal Transparent Latch, Three-State, Inverting	20	MSI	3837	
CD54HC564F3A	CD54HCT564F3A	Octal D-Type Flip-Flop, Three-State, Inverting	20	MSI	3838	
CD54HC573F3A	CD54HCT573F3A	Octal Transparent Latch, Three-State	20	MSI	3839	
CD54HC574F3A	CD54HCT574F3A	Octal D-Type Flip-Flop, Three-State	20	MSI	3840	
CD54HC597F3A	-	8-Bit Shift Register with I/P Latch	16	MSI	3841	
CD54HC640F3A	CD54HCT640F3A	Octal Bus Transceiver, Three-State, Inverting	20	MSI	3842	
CD54HC646F3A	CD54HCT646F3A	Octal Bus Transceiver/Register, Three-State	24	MSI	3843	
CD54HC670F3A	CD54HCT670F3A	4 X 4 Register File, Three-State	16	MSI	3844	

Data Sheet AnswerFAX Document Listing (Continued)

TYPE NUMBER			(NOTE 1)		ANSWERFAX
CMOS LOGIC	TTL LOGIC	DESCRIPTION	OF LEADS	CLASSIFICATION	DOCUMENT NUMBER
CD54HC688F3A	CD54HCT688F3A	8-Bit Magnitude Comparator	20	MSI	3845
CD54HC4002F3A	-	Dual 4-Input NOR Gate	14	SSI	3846
CD54HC4015F3A	-	Dual 4-Bit Serial-In/Parallel-Out Shift Register	16	MSI	3847
CD54HC4017F3A	CD54HCT4017F3A	Johnson Decade Counter with 10 Decoded Outputs	16	MSI	3848
CD54HC4020F3A	CD54HCT4020F3A	14-Stage Binary Ripple Counter	16	MSI	3849
CD54HC4024F3A	CD54HCT4024F3A	7-Stage Binary Ripple Counter	14	MSI	3850
CD54HC4040F3A	CD54HCT4040F3A	12-Bit Binary Ripple Counter	16	MSI	3851
CD54HC4046AF3A	CD54HCT4046AF3A	Phase-Locked Loop with VCO	16	MSI	3852
CD54HC4049F3A	-	Hex Inverting HIGH-to-LOW Level Shifter	16	SSI	3853
CD54HC4050F3A	-	Hex HIGH-to-LOW Level Shifter	16	SSI	3854
CD54HC4051F3A	CD54HCT4051F3A	8-Channel Analog Multiplexer/Demultiplexer	16	MSI	3855
CD54HC4052F3A	CD54HCT4052F3A	Dual 4-Channel Analog Multiplexer/ Demultiplexer	16	MSI	3856
CD54HC4053F3A	CD54HCT4053F3A	Triple 2-Channel Analog Multiplexer/ Demultiplexer	16	MSI	3857
CD54HC4059F3A	CD54HCT4059F3A	Programmable Divided-by-"N" Counter	24	MSI	3858
CD54HC4060F3A	CD54HCT4060F3A	14-Stage Binary Ripple Counter with Oscillator	16	MSI	3859
CD54HC4066F3A	-	Quad Bilateral Switch	14	SSI	3860
CD54HC4075F3A	CD54HCT4075F3A	Triple 3-Input OR Gate	14	SSI	3861
CD54HC4094F3A	-	8-Stage Shift-and-Store Bus Register	16	MSI	3862
CD54HC4316F3A	-	Quad Analog Switch	16	MSI	3863
CD54HC4351F3A	-	Analog Multiplexer with Latch	20	MSI	3864
CD54HC4511F3A	-	BCD-to-7-Segment Latch/Decoder/Driver	16	MSI	3865
CD54HC4514F3A	-	4-to-16-Line Decoder/Demultiplexer with Input Latches	24	MSI	3866
CD54HC4515F3A	-	4-to-16-Line Decoder with Input Latches	24	MSI	3867
CD54HC4516F3A	-	Up/Down Counter, Binary	16	MSI	3868
CD54HC4520F3A	CD54HCT4520F3A	Dual 4-Bit Synchronous Binary Counter	16	MSI	3869
CD54HC4538F3A	CD54HCT4538F3A	Dual Precision Monostable Multivibrator	16	MSI	3870
CD54HC7266F3A	-	Quad Exclusive NOR	14	SSI	3871
-	CD54HCT40102F3A	8-Bit Synchronous BCD Down Counter	16	MSI	3872
CD54HC40103F3A	-	8-Bit Binary Down Counter	16	MSI	3873
CD54HC40105F3A	CD54HCT40105F3A	4-Bits X 16 Words FIFO Register	16	MSI	3874
CD54HCU04F3A	-	Hex Inverter (Unbuffered)	14	SSI	3875

NOTE:

^{1.} These lead counts are for dual-in-line packages only.



Harris SMD and DESC Parts List, Digital - Logic CD54HC/HCT

HARRIS DEVICE	MILITARY REFERENCE	DESCRIPTION
CD54HC00F3A	8403701CA	Quad 2-Input NAND Gate
CD54HC02F3A	8404101CA	Quad 2-Input NOR Gate
CD54HC03F3A	5962-8764701CA	Quad 2-Input NAND Gate with Open Drain
CD54HC04F3A	8409801CA	Hex Inverter
CD54HC08F3A	8404701CA	Quad 2-Input AND Gate
CD54HC10F3A	8403801CA	Triple 3-Input NAND Gate
CD54HC11F3A	8404801CA	Triple 3-Input AND Gate
CD54HC14F3A	8409101CA	Hex Inverting Schmitt Trigger
CD54HC20F3A	8403901CA	Dual 4-Input NAND Gate
CD54HC21F3A	5962-8857601CA	Dual 4-Input AND Gate
CD54HC27F3A	8404201CA	Triple 3-Input NOR Gate
CD54HC30F3A	8404001CA	8-Input NAND Gate
CD54HC32F3A	8404501CA	Quad 2-Input OR Gate
CD54HC42F3A	5962-8682101EA	BCD-to-Decimal Decoder (1-to-10)
CD54HC73F3A	5962-8515301CA	Dual J-K Flip-Flop with Reset
CD54HC74F3A	8405601CA	Dual D Flip-Flop with Set and Reset
CD54HC75F3A	8407001EA	Quad Bistable Transparent Latch
CD54HC85F3A	8601301EA	4-Bit Magnitude Comparator
CD54HC86F3A	8404601CA	Quad 2-Input Exclusive OR Gate
CD54HC107F3A	5962-8515401CA	Dual J-K Flip-Flop with Reset
CD54HC109F3A	8415001EA	Dual J-K Flip-Flop with Set and Reset
CD54HC112F3A	8408801EA	Dual J-K Flip-Flop with Set and Reset
CD54HC123F3A	5962-8684701EA	Dual Retriggerable Monostable Multivibrator with Reset

Harris SMD and DESC Parts List, Digital - Logic CD54HC/HCT (Continued)

HARRIS DEVICE	MILITARY REFERENCE	DESCRIPTION
CD54HC125F3A	5962-8772101CA	Quad Three-State Buffer
CD54HC126F3A	5962-8684801CA	Quad Three-State Buffer
CD54HC138F3A	8406201EA	3-to-8-Line Decoder/Demultiplexer, Inverting
CD54HC139F3A	8409201EA	Dual 2-of-4-Line Decoder/Demultiplexer
CD54HC147F3A	8406401EA	10-to-4-Line Priority Encoder
CD54HC151F3A	8412801EA	8-Input Multiplexer
CD54HC153F3A	8409301EA	Dual 4-Input Multiplexer
CD54HC154F3A	5962-8682201JA	4-to-16-Line Decoder/Demultiplexer
CD54HC157F3A	5962-8606101EA	Quad 2-Input Multiplexer
CD54HC158F3A	5962-8682301EA	Quad 2-Input Multiplexer Inverting
CD54HC160F3A	5962-8682401EA	Synchronous BCD Decade Counter, Asynchronous Reset
CD54HC161F3A	8407501EA	Synchronous 4-Bit Binary Counter, Asynchronous Reset
CD54HC162F3A	8409401EA	Synchronous BCD Decade Counter, Synchronous Reset
CD54HC163F3A	8607601EA	Synchronous 4-Bit Binary Counter, Synchronous Reset
CD54HC164F3A	8416201CA	8-Bit Serial-In/Parallel-Out Shift Register
CD54HC165F3A	8409501EA	8-Bit Parallel-In/Serial-Out Shift Register
CD54HC173F3A	5962-8682501EA	Quad D-Type Flip-Flop, Three-State
CD54HC174F3A	8407301EA	Hex D-Type Flip-Flop with Reset
CD54HC175F3A	8408901EA	Quad D-Type Flip-Flop with Reset
CD54HC190F3A	5962-8994601EA	Presettable SYN BCD Up/Down Counter
CD54HC191F3A	5962-8689101EA	Synchronous 4-Bit Binary Up/Down Counter
CD54HC192F3A	5962-8780801EA	Synchronous BCD Decade Up/Down Counter
CD54HC193F3A	5962-8772401EA	Synchronous 4-Bit Binary Up/Down Counter
CD54HC194F3A	5962-8682601EA	4-Bit Bidirectional Universal Shift Register
CD54HC195F3A	5962-8682701EA	4-Bit Parallel Access Shift Register
CD54HC221F3A	5962-8780501EA	Dual Monostable Multivibrator with Reset
CD54HC237F3A	5962-8860601EA	3-to-8-Line Decoder with Latch
CD54HC238F3A	5962-8688401EA	3-to-8-Line Decoder/Demultiplexer
CD54HC240F3A	8407401RA	Octal Buffer/Line Driver, Three-State, Inverting
CD54HC243F3A	8409001CA	Quad Bus Transceiver, Three-State
CD54HC244F3A	8409601RA	Octal Buffer/Line Driver, Three-State
CD54HC245F3A	8408501RA	Octal Bus Transceiver, Three-State
CD54HC251F3A	8512501EA	8-Input Multiplexer, Three-State
CD54HC257F3A	8512401EA	Quad 2-Input Multiplexer, Three-State
CD54HC259F3A	8551901EA	8-Bit Addressable Latch
CD54HC273F3A	8409901RA	Octal D-Type Flip-Flop with Reset
CD54HC280F3A	8607701CA	9-Bit Odd/Even Parity Generator/Checker
CD54HC283F3A	5962-8976501EA	4-Bit Binary Full Adder with Fast Carry
CD54HC297F3A	5962-8999001EA	Digital Phase-Locked-Loop
CD54HC299F3A	5962-8780601RA	8-Bit Universal Shift Register, Three-State
CD54HC365F3A	8500101EA	Hex Buffer/Line Driver, Three-State
CD54HC366F3A	5962-8682801EA	Hex Buffer/Line Driver, Three-State, Inverting
CD54HC367F3A	8500201EA	Hex Buffer/Line Driver, Three-State

Harris SMD and DESC Parts List, Digital - Logic CD54HC/HCT (Continued)

HARRIS DEVICE	MILITARY REFERENCE	DESCRIPTION
CD54HC368F3A	5962-8681201EA	Hex Buffer/Line Driver, Three-State, Inverting
CD54HC373F3A	8407201RA	Octal Transparent Latch, Three-State
CD54HC374F3A	8407101RA	Octal D-Type Flip-Flop, Three-State
CD54HC377F3A	5962-8780701RA	Octal D-Type Flip-Flop with Data Enable
CD54HC393F3A	8410001CA	Dual 4-Bit Binary Ripple Counter
CD54HC533F3A	5962-8681301RA	Octal Transparent Latch, Three-State, Inverting
CD54HC534F3A	5962-8681401RA	Octal D-Type Flip-Flop, Three-State, Inverting
CD54HC563F3A	5962-8606201RA	Octal Transparent Latch, Three-State, Inverting
CD54HC564F3A	5962-8681501RA	Octal D-Type Flip-Flop, Three-State, Inverting
CD54HC573F3A	8512801RA	Octal Transparent Latch, Three-State
CD54HC597F3A	5962-8681701EA	8-Bit Shift Register with I/P Latch
CD54HC640F3A	5962-8780901RA	Octal Bus Transceiver, Three-State Inverting
CD54HC646F3A	5962-8688501JA	Octal Bus Transceiver/Register, Three-State
CD54HC688F3A	5962-8681801RA	8-Bit Magnitude Comparator
CD54HC4002F3A	8404401CA	Dual 4-Input NOR Gate
CD54HC4015F3A	5962-8995301EA	Dual 4-Bit Serial-In/Parallel-Out Shift Register
CD54HC4017F3A	8601101EA	Johnson Decade Counter with 10 Decoded Outputs
CD54HC4020F3A	8500301EA	14-Stage Binary Ripple Counter
CD54HC4024F3A	8601201CA	7-Stage Binary Ripple Counter
CD54HC4040F3A	8500401EA	12-Bit Binary Ripple Counter
CD54HC4046AF3A	5962-8960901EA	Phase-Locked Loop with VCO
CD54HC4049F3A	5962-8681901EA	Hex Inverting HIGH-to-LOW Level Shifter
CD54HC4050F3A	5962-8682001EA	Hex HIGH-to-LOW Level Shifter
CD54HC4052F3A	5962-8855601EA	Dual 4-Channel Analog Multiplexer/Demultiplexer
CD54HC4053F3A	5962-8775401EA	Triple 2-Channel Analog Multiplexer/Demultiplexer
CD54HC4059F3A	5962-8944501JA	Programmable Divide by "N" Counter
CD54HC4060F3A	5962-8768001EA	14-Stage Binary Ripple Counter with Oscillator
CD54HC4066F3A	5962-8950701CA	Quad Bilateral Switch
CD54HC4075F3A	5962-8772201CA	Triple 3-Input OR Gate
CD54HC4511F3A	5962-8773301EA	BCD-to-7 Segment Latch/Decoder/Driver
CD54HC4520F3A	5962-8995401EA	Dual 4-Bit Synchronous Binary Counter
CD54HC4538F3A	5962-8688601EA	Dual Precision Monostable Multivibrator
CD54HC7266F3A	8404302CA	Quad Exclusive NOR
CD54HC40103F3A	5962-9055301EA	8-Bit Binary Down Counter
CD54HCT00F3A	5962-8683101CA	Quad 2-Input NAND Gate
CD54HCT02F3A	5962-8975101CA	Quad 2-Input NOR Gate
CD54HCT04F3A	5962-8974701CA	Hex Inverter
CD54HCT08F3A	5962-8688301CA	Quad 2-Input AND Gate
CD54HCT10F3A	5962-8984301CA	Triple 3-Input NAND Gate
CD54HCT11F3A	5962-8970901CA	Triple 3-Input AND Gate
CD54HCT14F3A	5962-8689001CA	Hex Inverting Schmitt Trigger
CD54HCT27F3A	5962-8970301CA	Triple 3-Input NOR Gate

Harris SMD and DESC Parts List, Digital - Logic CD54HC/HCT (Continued)

HARRIS DEVICE	MILITARY REFERENCE	DESCRIPTION
CD54HCT30F3A	5962-8974601CA	8-Input NAND
CD54HCT32F3A	5962-8685201CA	Quad 2-Input OR Gate
CD54HCT74F3A	5962-8685301CA	Dual D Flip-Flop with Set and Reset
CD54HCT75F3A	5962-9075801MEA	Quad Bistable Transparent Latch
CD54HCT85F3A	5962-8867201EA	4-Bit Magnitude Comparator
CD54HCT86F3A	5962-8984401CA	Quad 2-Input Exclusive OR Gate
CD54HCT107F3A	5962-9084901MCA	Dual J-K Flip-Flop with Reset
CD54HCT109F3A	5962-9070101MEA	Dual J-K Flip-Flop with Set and Reset
CD54HCT112F3A	5962-8970201EA	Dual J-K Flip-Flop with Set and Reset
CD54HCT123F3A	5962-8970001EA	Dual Retriggerable Monostable Multivibrator with Set and Reset
CD54HCT126F3A	5962-9065101MCA	Quad Three-State Buffer
CD54HCT132F3A	5962-8984501CA	Quad 2-Input NAND Schmitt TrIgger
CD54HCT138F3A	8550401EA	3-to-8-Line Decoder/Demultiplexer, Inverting
CD54HCT151F3A	5962-9065201MEA	8-Input Multiplexer
CD54HCT153F3A	5962-9050501MEA	Dual 4-Input Multiplexer
CD54HCT154F3A	5962-8670101JA	4-to-16-Line Decoder/Demultiplexer
CD54HCT157F3A	5962-9070201MEA	Quad 2-Input Multiplexer
CD54HCT158F3A	5962-9070301MEA	Quad 2-Input Multiplexer, Inverting
CD54HCT160F3A	5962-9070501MEA	Synchronous BCD Decade Counter, Asynchronous Reset
CD54HCT161F3A	5962-8685401EA	Synchronous 4-Bit Binary Counter, Asynchronous Reset
CD54HCT162F3A	5962-8970701EA	Synchronous BCD Decade Counter, Asynchronous Reset
CD54HCT164F3A	5962-8970401CA	8-Bit Serial-In/Parallel-Out Shift Register
CD54HCT165F3A	5962-8685501EA	8-Bit Parallel-In/Serial-Out Shift Register
CD54HCT173F3A	5962-8875901EA	Quad D-Type Flip-Flop, Three-State
CD54HCT174F3A	5962-8974301EA	Hex D-Type Flip-Flop with Reset
CD54HCT175F3A	5962-8970101EA	Quad D-Type Flip-Flop with Reset
CD54HCT191F3A	5962-8867101EA	Synchronous 4-Bit Binary Up/Down Counter
CD54HCT193F3A	5962-9084801MEA	Synchronous 4-Bit Binary Up/Down Counter
CD54HCT238F3A	5962-8974501EA	3-to-8-Line Decoder/Demultiplexer
CD54HCT240F3A	8550501RA	Octal Buffer/Line Driver, Three-State, Inverting
CD54HCT244F3A	8513001RA	Octal Buffer/Line Driver, Three-State
CD54HCT245F3A	8550601RA	Octal Buffer Transceiver, Three-State
CD54HCT251F3A	5962-9052401MEA	8-Input Multiplexer, Three-State
CD54HCT257F3A	5962-8970501EA	Quad 2-Input Multiplexer, Three-State
CD54HCT258F3A	5962-8970801EA	Quad 2-Line-to-4-Line Data Selector
CD54HCT259F3A	5962-8985201EA	8-Bit Addressable Latch
CD54HCT273F3A	5962-8772501RA	Octal D-Type Flip-Flop with Reset
CD54HCT299F3A	5962-8943601MRA	8-Bit Universal Shift Register, Three-State
CD54HCT367F3A	5962-9070601MEA	Hex Buffer/Line Driver, Three-State
CD54HCT373F3A	5962-8686701RA	Octal Transparent Latch, Three-State
CD54HCT374F3A	8550701RA	Octal D-Type Flip-Flop, Three-State
CD54HCT377F3A	5962-8976901RA	Octal D-Type Flip-Flop with Data Enable

Harris SMD and DESC Parts List, Digital - Logic CD54HC/HCT (Continued)

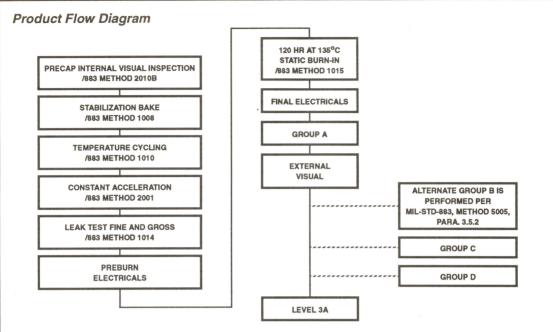
HARRIS DEVICE	MILITARY REFERENCE	DESCRIPTION
CD54HCT390F3A	5962-9098401MEA	Dual Decade Ripple Counter
CD54HCT393F3A	5962-8989001CA	Dual 4-Bit Binary Ripple Counter
CD54HCT534F3A	5962-8984901RA	Octal D-Type Flip-Flop, Three-State, Inverting
CD54HCT573F3A	5962-8685601RA	Octal Transparent Latch, Three-State
CD54HCT574F3A	5962-8974201RA	Octal D-Type Flip-Flop, Three-State
CD54HCT640F3A	5962-8974001RA	Octal Bus Transceiver, Three-State, Inverting
CD54HCT688F3A	5962-8685701RA	8-Bit Magnitude Comparator
CD54HCT4017F3A	5962-9059701MEA	Johnson Decade Counter with 10 Decoded Outputs
CD54HCT4020F3A	5962-8945801EA	14-Stage Binary Ripple Counter
CD54HCT4040F3A	5962-8994701MEA	12-Bit Binary Ripple Counter
CD54HCT4046AF3A	5962-8875701EA	Phase-Lock Loop with VCO
CD54HCT4051F3A	5962-9065401MEA	8-Channel Analog Multiplexer/Demultiplexer
CD54HCT4052F3A	5962-9163001MEA	Dual 4-Channel Analog Multiplexer/Demultiplexer
CD54HCT4059F3A	5962-8862401JA	Programmable Divided-by-N Counter
CD54HCT4060F3A	5962-8977101EA	14-Stage Binary Ripple Counter with Oscillator
CD54HCT40102F3A	5962-9057401EA	8-Bit Synchronous BCD Down Counter
CD54HCU04F3A	8601001CA	Hex Inverter (Unbuffered)

Lot Screening Tests Total Lot Screening (X = 100% Testing)

		MIL-	STD-883	SCREENING	
SCREENING TESTS	TEST CONDITIONS	METHOD	CONDITIONS	LEVEL 3A	NOTES
ASSEMBLY			Considerated by Coder Expension Constant in Codebas		
Precap Visual		2010	В	Х	-
PRECONDITIONING			***************************************		
Stabilization Bake	24 Hrs Min at 200°C	1008	D	Х	
Temperature Cycling	10 Cycles	1010	С	X	-65°C/150°C
Centrifuge	Y ₁ Direction Only	2001	E	×	30,000 Gs
Fine Leak		1014	A or B	Х	5 x 10 ⁻⁸ Reject Limit
Gross Leak		1014	С	X	-
TEST AND BURN-IN			***************************************		
Initial Test		-		Х	-
Static Burn-In II	120 Hrs at 135°C	1015	В	х	1, 3
FINAL ELECTRICAL					
DC Electrical	+25°C			×	2
	-55°C			Х	-
	+125°C		-	Х	-
AC Electrical	+25°C			Х	-

NOTES:

- 1. Alternate time/temperature regression used per Method 1015. All inputs at V_{CC} ; outputs open.
- 2. All electrical testing per parameters shown in individual device data sheets.
- 3. PDA = 5%, one reburn allowed at 3%.



HARRIS HIGH-RELIABILITY LEVEL 3A 54HC/HCT ICs MIL-STD-883, CLASS B COMPLIANT

Transistor Count Per Device

DEVICE TYPE	TRANSISTORS
CD54HC00F3A	40
CD54HC02F3A	72
CD54HC03F3A	76
CD54HC04F3A	36
CD54HC08F3A	32
CD54HC10F3A	51
CD54HC11F3A	66
CD54HC14F3A	90
CD54HC20F3A	28
CD54HC21F3A	40
CD54HC27F3A	87
CD54HC30F3A	40
CD54HC32F3A	32
CD54HC42F3A	124
CD54HC73F3A	126
CD54HC74F3A	96
CD54HC75F3A	80
CD54HC85F3A	208
CD54HC86F3A	96
CD54HC107F3A	118
CD54HC109F3A	128
CD54HC112F3A	134
CD54HC123F3A	188
CD54HC125F3A	80

DEVICE TYPE	TRANSISTORS
CD54HC126F3A	88
CD54HC132F3A	104
CD54HC138F3A	132
CD54HC139F3A	96
CD54HC147F3A	178
CD54HC151F3A	126
CD54HC153F3A	112
CD54HC154F3A	250
CD54HC157F3A	104
CD54HC158F3A	114
CD54HC160F3A	306
CD54HC161F3A	330
CD54HC162F3A	302
CD54HC163F3A	282
CD54HC164F3A	212
CD54HC165F3A	368
CD54HC166F3A	266
CD54HC173F3A	294
CD54HC174F3A	184
CD54HC175F3A	152
CD54HC190F3A	502
CD54HC191F3A	380
CD54HC192F3A	/ 262
CD54HC193F3A	240

DEVICE TYPE	TRANSISTORS
CD54HC194F3A	250
CD54HC195F3A	188
CD54HC221F3A	332
CD54HC237F3A	172
CD54HC238F3A	148
CD54HC240F3A	112
CD54HC243F3A	166
CD54HC244F3A	112
CD54HC245F3A	114
CD54HC251F3A	154
CD54HC253F3A	106
CD54HC257F3A	90
CD54HC259F3A	256
CD54HC273F3A	254
CD54HC280F3A	180
CD54HC283F3A	194
CD54HC297F3A	1040
CD54HC299F3A	414
CD54HC354F3A	224
CD54HC356F3A	446
CD54HC365F3A	128
CD54HC366F3A	140
CD54HC367F3A	128
CD54HC368F3A	140

Transistor Count Per Device (Continued)

DEVICE TYPE	TRANSISTORS
CD54HC373F3A	188
CD54HC374F3A	234
CD54HC377F3A	294
CD54HC393F3A	188
CD54HC533F3A	264
CD54HC534F3A	218
CD54HC540F3A	106
CD54HC541F3A	138
CD54HC563F3A	264
CD54HC564F3A	304
CD54HC573F3A	154
CD54HC574F3A	260
CD54HC597F3A	520
CD54HC640F3A	106
CD54HC646F3A	830
CD54HC670F3A	464
CD54HC688F3A	60
CD54HC4002F3A	56
CD54HC4015F3A	252
CD54HC4017F3A	254
CD54HC4020F3A	336
CD54HC4024F3A	176
CD54HC4040F3A	294
CD54HC4046AF3A	248
CD54HC4049F3A	36
CD54HC4050F3A	24
CD54HC4051F3A	304
CD54HC4052F3A	200
CD54HC4053F3A	230
CD54HC4059F3A	1400
CD54HC4060F3A	332
CD54HC4066F3A	56
CD54HC4075F3A	54
CD54HC4094F3A	300
CD54HC4316F3A	160
CD54HC4351F3A	230
CD54HC4511F3A	251
CD54HC4514F3A	344
CD54HC4515F3A	312
CD54HC4516F3A	348
CD54HC4520F3A	268
CD54HC4538F3A	172
CD54HC7266F3A	48
CD54HC40103F3A	642
CD54HC40105F3A	694
CD54HCU04F3A	12
CD54HCT00F3A	72

DEVICE TYPE	TRANSISTORS
CD54HCT02F3A	72
CD54HCT03F3A	76
CD54HCT04F3A	48
CD54HCT08F3A	80
CD54HCT10F3A	78
CD54HCT11F3A	102
CD54HCT14F3A	114
CD54HCT20F3A	80
CD54HCT21F3A	72
CD54HCT27F3A	87
CD54HCT30F3A	40
CD54HCT32F3A	72
CD54HCT42F3A	134
CD54HCT74F3A	100
CD54HCT75F3A	80
CD54HCT85F3A	224
CD54HCT86F3A	96
CD54HCT107F3A	130
CD54HCT109F3A	134
CD54HCT112F3A	164
CD54HCT123F3A	196
CD54HCT125F3A	96
CD54HCT126F3A	104
CD54HCT132F3A	128
CD54HCT138F3A	132
CD54HCT139F3A	116
CD54HCT151F3A	126
CD54HCT153F3A	160
CD54HCT154F3A	258
CD54HCT157F3A	124
CD54HCT158F3A	132
CD54HCT160F3A	338
CD54HCT161F3A	340
CD54HCT162F3A	338
CD54HCT163F3A	294
CD54HCT164F3A	228
CD54HCT165F3A	368
CD54HCT166F3A	266
CD54HCT173F3A	294
CD54HCT174F3A	188
CD54HCT175F3A	156
CD54HCT191F3A	404
CD54HCT193F3A	252
CD54HCT194F3A	250
CD54HCT238F3A	148
CD54HCT240F3A	96
CD54HCT241F3A	110

DEVICE TYPE	TRANSISTORS
CD54HCT243F3A	166
CD54HCT244F3A	132
CD54HCT245F3A	114
CD54HCT251F3A	154
CD54HCT257F3A	90
CD54HCT258F3A	84
CD54HCT259F3A	256
CD54HCT273F3A	254
CD54HCT280F3A	180
CD54HCT283F3A	228
CD54HCT299F3A	414
CD54HCT365F3A	128
CD54HCT366F3A	160
CD54HCT367F3A	156
CD54HCT373F3A	188
CD54HCT374F3A	234
CD54HCT377F3A	300
CD54HCT390F3A	264
CD54HCT393F3A	188
CD54HCT423F3A	194
CD54HCT533F3A	264
CD54HCT534F3A	252
CD54HCT541F3A	178
CD54HCT564F3A	264
CD54HCT573F3A	160
CD54HCT574F3A	260
CD54HCT640F3A	106
CD54HCT646F3A	830
CD54HCT670F3A	464
CD54HCT688F3A	60
CD54HCT4017F3A	254
CD54HCT4020F3A	344
CD54HCT4024F3A	180
CD54HCT4040F3A	302
CD54HCT4046AF3A	248
CD54HCT4051F3A	308
CD54HCT4052F3A	209
CD54HCT4053F3A	230
CD54HCT4059F3A	1400
CD54HCT4060F3A	340
CD54HCT4075F3A	54
CD54HCT4520F3A	268
CD54HCT4538F3A	172
CD54HCT40102F3A	650
CD54HCT40105F3A	694

Absolute Maximum Ratings

DC Supply Voltage, V _{CC}	Power Dissipation Per Package, P _D
(Voltages Referenced to Ground)0.5 to +7.0V	Package F
DC Input Voltage Range, All Inputs, V _{IN} 0.5 to V _{CC} +0.5V	$T_A = -55^{\circ}C \text{ to } +100^{\circ}C \dots 500 \text{mW}$
DC Output Voltage Range, All Outputs, VOLT0.5 to VCC +0.5V	$T_A = +100$ °C to $+125$ °C Derate Linearly at 8mW/°C to 300mW
DC Input Diode Current, I _{IK}	Operating Temperature Range, T _A 55°C to +125°C
For V _I < -0.5V or V _I > V _{CC} + 0.5V	Storage Temperature, T _{STG} 65°C to +150°C
DC Output Diode Current, IOK	Lead Temperature (During Soldering)
For $V_0 < -0.5V$ or $V_0 > V_{CC} + 0.5V$ ±20mA	At Distance 1/16in. ± 1/32in. (1.59mm ± 0.79mm)
DC Drain Current, Per Output, I _O	From Case For 10s Max
For -0.5V < V _O < V _{CC} + 0.5V	Unit Inserted into a PC Board (Min Thickness 1/16in., 1.59mm)
Standard Output	with Solder Contacting Lead Tips Only +300°C
Bus Driver Output	
DC V _{CC} or Ground Current, I _{CC}	
Standard Output	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

Supply Voltage Range, V _{CC}	Operating Temperature, T _A 55°C to +125°C
For T _A = Full Package Temperature Range	Input Rise and Fall Time, t _R , t _F
CD54HC Types	2V
CD54HCT Types	4.5V
DC Input or Output Voltage, V _{IN} , V _{OUT} 0 to V _{CC}	6V

Standard DC Electrical Specifications - CD54HC Series

Non-standard DC Electrical Specifications are included in individual data sheets.

				TEST C	ONDITIO	NS	T _A = -	-25°C	T _A = -55°C TO +125°C		
PARAMETERS		SYMBOL	V _{IN} (V)			V _{CC} (V)	MIN	MAX	MIN	MAX	UNITS
High Level Input Voltage		V _{IH}				2	1.5	-	1.5	-	V
						4.5	3.15 (Note 1)	-	3.15 (Note 1)	-	٧
						6	4.2	-	4.2	-	V
Low Level Input Voltage		V _{IL}				2	-	0.5	-	0.5	V
						4.5	-	1.35 (Note 1)	-	1.35 (Note 1)	٧
						6	-	1.8	-	1.8	٧
High Level Output Voltage	CMOS	V _{OH}	V _{IL}	I _O = -	20μΑ	2	1.9	-	1.9	-	V
	Loads		or V _{IH}			4.5	4.4 (Note 1)	-	4.4 (Note 1)	-	٧
7						6	5.9	-	5.9	-	V
	TTL Loads (Table 1)	V _{OH}	V _{IL} or V _{IH}	STD -4	mA) BUS -6	4.5	3.98 (Note 1)	-	3.7 (Note 1)	-	V
				-5.2	-7.8	6	5.48	-	5.2	-	V
Low Level Output Voltage	CMOS	V _{OL}	V _{IL}	I _O = 2	20μΑ	2	-	0.1	-	0.1	٧
	Loads		or V _{IH}			4.5	-	0.1 (Note 1)	-	0.1 (Note 1)	٧
						6	-	0.1	-	0.1	٧
	TTL Loads (Table 1)		V _{IL} or V _{IH}	I _O (I STD 4	BUS	4.5	-	0.26 (Note 1)	-	0.4 (Note 1)	٧
				5.2	7.8	6		0.26	·	0.4	V

For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX.
 See Section 8, "How to use AnswerFAX", in this selection guide.
 6-15

Standard DC Electrical Specifications - CD54HC Series (Continued)

Non-standard DC Electrical Specifications are included in individual data sheets.

				TEST CONDITIONS			T _A = +25°C		$T_A = -55^{\circ}C \text{ TO } +125^{\circ}C$	
PARAMETE	RS	SYMBOL	V _{IN} (V)		V _{CC} (V)	MIN	MAX	MIN	MAX	UNITS
Input Leakage Current		I _{IN}	V _{CC} or GND		6	-	±0.1 (Note 1)		±1.0 (Note 1)	μА
Quiescent Supply Current	SSI	Icc	V _{CC}	I _{OUT} = 0	6	-	2 (Note 1)	-	40 (Note 1)	μА
(Note 2)	FF		GND		6	-	4 (Note 1)	-	80 (Note 1)	μА
	MSI				6	-	8 (Note 1)	-	160 (Note 1)	μА
Three-State Leakage Cu (Note 3)	rrent	loz	V _{IL} or V _{IH}	V _O = V _{CC} or GND	6	-	±0.5 (Note 1)	-	±10 (Note 1)	μА

NOTES:

- 1. These limits are tested 100%.
- 2. Listed in individual data sheets.
- 3. Individual data sheets will indicate where applicable.

Standard DC Electrical Specifications - CD54HCT Series

Non-standard DC Electrical Specifications are included in individual data sheets.

				TEST C	ONDITIC	NS	T _A = -	-25°C	T _A = -55 +12	5°C TO 5°C	
PARAMETE	RS	SYMBOL	V _{IN} (V)			V _{cc} (V)	MIN	MAX	MIN	MAX	UNITS
High Level Input Voltage		V _{IH}				4.5	2 (Note 1)	-	2 (Note 1)	-	٧
						5.5	2	-	2	-	V
Low Level Input Voltage		V _{IL}				4.5	-	0.8 (Note 1)	-	0.8 (Note 1)	V
						5.5	-	0.8	-	0.8	٧
High Level Output Voltage	CMOS Loads	V _{OH}	V _{IL} or V _{IH}	I _O = -	20μΑ	4.5	4.4 (Note 1)	-	4.4 (Note 1)	-	V
	TTL Loads (Table 1)		V _{IL} or V _{IH}	I _O (STD	mA) BUS -6	4.5	3.98	-	3.7	-	V
				· ·		1.0	(Note 1)		(Note 1)		ı '
Low Level Output Voltage	CMOS Loads	V _{OL}	V _{IL} or V _{IH}	I _O = 3	20μΑ	4.5	-	0.1 (Note 1)	-	0.1 (Note 1)	V
,	TTL Loads (Table 1)		V _{IL} or V _{IH}	l _o (mA) BUS						
			V IH	4	6	4.5	-	0.26 (Note 1)	-	0.4 (Note 1)	٧
Input Leakage Current		I _{IN}	V _{CC} or GND			6	-	±0.1 (Note 1)	-	±1.0 (Note 1)	μА

For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX. See Section 8, "How to use AnswerFAX", in this selection guide.

6-16

Standard DC Electrical Specifications - CD54HCT Series (Continued)

Non-standard DC Electrical Specifications are included in individual data sheets.

				TEST CONDITIONS		T _A = +25°C		T _A = -55°C TO +125°C		
PARAME	TERS	SYMBOL	V _{IN} (V)		V _{CC} (V)	MIN	MAX	MIN	MAX	UNITS
Quiescent Supply Current	SSI	Icc	V _{CC} or	I _{OUT} = 0	6	-	2 (Note 1)	-	40 (Note 1)	μА
(Note 2)	FF		GND		6	-	4 (Note 1)		80 (Note 1)	μА
	MSI				6	-	8 (Note 1)	-	160 (Note 1)	μА
Three-State Leakage (Note 3)	Current	l _{oz}	V _{IL} or V _{IH}	V _O = V _{CC} or GND	6	-	±0.5 (Note 1)	-	±10 (Note 1)	μА

NOTES:

- 1. These limits are tested 100%.
- 2. Listed in individual data sheets.
- 3. Individual data sheets will indicate where applicable.

Table 1. Standard TTL Output Load Characteristics - CD54HC/HCT Series (Note 1)

			TEST CONDITIONS							
						V	IN			
				нс/нст		HC	HCT	LIM	ITS	
PARAMETERS	SYMBOL	TEMP	V _{cc}	V _O	lo	V _{IL} OR V _{IH}	V _{IL} OR V _{IH}	MIN	MAX	UNITS
Output High (Source) Current, TTL Load	I _{OH}	+25°C	4.5	3.98	-	0, 4.5	0, 4.5	-4 (Note 2)	-	mA
		-55°C	4.5	3.70	-	0, 4.5	0, 4.5	-4 (Note 2)	-	mA
		+125°C	4.5	3.70	-	0, 4.5	0, 4.5	-4 (Note 2)	-	mA
Output Low (Sink) Current, TTL Load	loL	+25°C	4.5	0.26	-	0, 4.5	0, 4.5	4 (Note 2)	-	mA
		-55°C	4.5	0.40	-	0, 4.5	0, 4.5	4 (Note 2)	-	mA
		+125°C	4.5	0.40	-	0, 4.5	0, 4.5	4 (Note 2)	-	mA
High Level Output Voltage, TTL Load	V _{OH}	+25°C	4.5	-	-4	1.35, 3.15	0.8, 2.0	3.98 (Note 2)	-	٧
		-55°C	4.5	-	-4	1.35, 3.15	0.8, 2.0	3.70 (Note 2)	-	٧
		+125°C	4.5	-	-4	1.35, 3.15	0.8, 2.0	3.70 (Note 2)	-	٧
Low Level Output Voltage, TTL Load	V _{OL}	+25°C	4.5	-	4	1.35, 3.15	0.8, 2.0	-	0.26 (Note 2)	٧
		-55°C	4.5	-	4	1.35, 3.15	0.8, 2.0	-	0.40 (Note 2)	V
		+125°C	4.5	-	4	1.35, 3.15	0.8, 2.0	-	0.40 (Note 2)	٧

NOTES:

- 1. Individual data sheets will indicate the non-standard bus-driver types which will display different TTL output load characteristics.
- 2. These limits are tested 100%.

[‡] For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX. See Section 8, "How to use AnswerFAX", in this selection guide.

Advanced CMOS Logic ICs - AC/ACT Series

Guide to the Reliability Class and Package of Harris High-Reliability CD54AC/ACT ICs

CD54ACT00 SCREENING LEVEL PACKAGE DESIGNATION Dual-In-Line Ceramic 3A = Class B, MIL-STD-883 Compliant

HARRIS DEVICE PART NUMBER

AC = CMOS Compatible ACT = TTL Compatible

(CerDIP)

Data Sheet AnswerFAX Document Listing

CMOS COMPATIBLE LOGIC	TTL COMPATIBLE LOGIC		NUMBER		ANSWERFAX DOCUMENT
CERDIP	CERDIP	DESCRIPTION	OF LEADS	CLASSIFICATION	NUMBER
CD54AC00F3A	CD54ACT00F3A	Quad 2-Input NAND Gate	14	SSI	3876
CD54AC02F3A	CD54ACT02F3A	Quad 2-Input NOR Gate	14	SSI	3877
CD54AC04F3A	CD54ACT04F3A	Hex Inverter/Buffer	14	SSI	3878
CD54AC05F3A	CD54ACT05F3A	Hex Inverter/Buffer, Open-Drain Outputs	14	SSI	3879
CD54AC08F3A	CD54ACT08F3A	Quad 2-Input AND Gate	14	SSI	3880
-	CD54ACT20F3A	Dual 4-Input NAND Gate	14	SSI	3881
CD54AC32F3A	CD54ACT32F3A	Quad 2-Input OR Gate	14	SSI	3882
CD54AC74F3A	CD54ACT74F3A	Dual D Flip-Flop with Set and Reset	14	FF	3883
-	CD54ACT86F3A	Quad 2-Input Exclusive-OR Gate	14	SSI	3884
CD54AC109F3A	CD54ACT109F3A	Dual J-K Flip-Flop with Set and Reset	16	FF	3885
CD54AC112F3A	CD54ACT112F3A	Dual J-K Flip-Flop with Set and Reset	16	FF	3886
CD54AC138F3A	CD54ACT138F3A	3-to-8-Line Decoder/Demultiplexer, Inverting	16	MSI	3887
CD54AC139F3A	CD54ACT139F3A	Dual 2-to-4-Line Decoder/ Demultiplexer	16	MSI	3888
-	CD54ACT151F3A	8-Input Multiplexer	16	MSI	3889
CD54AC153F3A	CD54ACT153F3A	Dual 4-Input Multiplexer	16	MSI	3890
CD54AC157F3A	-	Quad 2-Input Multiplexer	16	MSI	3891
CD54AC161F3A	CD54ACT161F3A	Synchronous 4-Bit Binary Counter, Asynchronous Reset	16	MSI	3892
CD54AC163F3A	CD54ACT163F3A	Synchronous 4-Bit Binary Counter, Synchronous Reset	16	MSI	3893
CD54AC164F3A	CD54ACT164F3A	8-Bit Serial-In Parallel-Out Shift Register	14	MSI	3894
-	CD54ACT174F3A	Hex D-Type Flip-Flop with Reset	16	MSI	3895
CD54AC191F3A	CD54ACT191F3A	Synchronous 4-Bit Binary Up/Down Counter	16	MSI	3896
CD54AC193F3A	CD54ACT193F3A	Synchronous 4-Bit Binary Up/Down Counter	16	MSI	3897
CD54AC240F3A	CD54ACT240F3A	Octal Buffer/Line Driver, Three-State, Inverting	20	MSI	3898
-	CD54ACT241F3A	Octal-Buffer/Line Driver, Three-State	20	MSI	3899
CD54AC244F3A	CD54ACT244F3A	Octal-Buffer/Line Driver, Three-State	20	MSI	3900
CD54AC245F3A	CD54ACT245F3A	Octal-Bus Transceiver, Three-State	20	MSI	3901
-	CD54ACT253F3A	Dual 4-Input Multiplexer, Three-State	16	MSI	3902

MILITARY GRADE/ 91 HIGH-RELIABILITY

Advanced CMOS Logic ICs - AC/ACT Series

Data Sheet AnswerFAX Document Listing (Continued)

CMOS COMPATIBLE LOGIC	TTL COMPATIBLE LOGIC		NUMBER		ANSWERFAX DOCUMENT
CERDIP	CERDIP	DESCRIPTION	OF LEADS	CLASSIFICATION	NUMBER
CD54AC257F3A	CD54ACT257F3A	Quad 2-Input Multiplexer, Three-State	16	MSI	3903
CD54AC273F3A	CD54ACT273F3A	Octal D-Type Flip-Flop with Reset	20	MSI	3904
CD54AC280F3A	CD54ACT280F3A	9-Bit Odd/Even Parity Generator/ Checker	14	MSI	3905
CD54AC283F3A	CD54ACT283F3A	4-Bit Full Adder with Fast Carry	16	MSI	3906
CD54AC299F3A	CD54ACT299F3A	8-Bit Universal Shift Register, Three-State	20	MSI	3907
-	CD54ACT323F3A	8-Bit Universal Shift Register, Three-State (with Synchronous Reset)	20	MSI	3908
CD54AC373F3A	CD54ACT373F3A	Octal Transparent Latch, Three-State,	20	MSI	3909
CD54AC374F3A	CD54ACT374F3A	Octal F Flip-Flop, Three-State	20	MSI	3910
-	CD54ACT533F3A	Octal Transparent Latch, Three-State, Inverting	20	MSI	3911
CD54AC534F3A	CD54ACT534F3A	Octal D Flip-Flop, Three-State, Inverting	20	MSI	3912
-	CD54ACT540F3A	Octal Buffer/Line Driver, Three-State, Inverting	20	MSI	3913
CD54AC541F3A	CD54ACT541F3A	Octal Buffer/Line Driver, Three-State	20	MSI	3914
CD54AC573F3A	CD54ACT573F3A	Octal Transparent Latch, Three-State	20	MSI	3915
CD54AC574F3A	CD54ACT574F3A	Octal D-Type Flip-Flop, Three-State	20	MSI	3916
•	CD54ACT623F3A	Octal Bus Transceiver, Three-State, Non-Inverting	20	MSI	3917

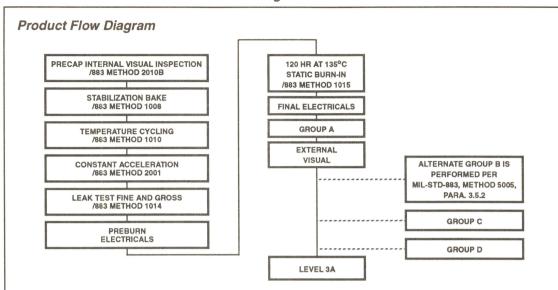
Lot Screening Tests Total Lot Screening (X = 100% Testing)

		MIL-	STD-883	SCREENING	
SCREENING TESTS	TEST CONDITIONS	METHOD	CONDITIONS	LEVEL 3A	NOTES
ASSEMBLY					
Precap Visual		2010	В	Х	-
PRECONDITIONING					
Stabilization Bake	24 Hrs Min at 200°C	1008	D	Х	•
Temperature Cycling	10 Cycles	1010	С	Х	-65°C/150°C
Centrifuge	Y ₁ Direction Only	2001	E	Х	30,000 Gs
Fine Leak		1014	A or B	Х	•
Gross Leak		1014	С	Х	-
TEST AND BURN-IN					
Initial Test			-	Х	-
Static Burn-In (Circuit II)	120 Hrs at 135°C	1015	В	Х	1
FINAL ELECTRICAL					
DC Electrical	+25°C		-	Х	2, 3
	-55°C		-	Х	•
	+125°C	-	-	Х	-
AC Electrical	+25°C, -55°C, +125°C	-	-	Х	-
Group A			X	Х	4

NOTES:

- 1. Alternate time/temperature regression used per Method 1015.
- 2. All electrical testing per parameters shown in individual device data sheets.
- 3. PDA = 5%, one reburn allowed at 3%.
- 4. Sample Test performed per Method 5005 of MIL-STD-883.

Advanced CMOS Logic ICs - AC/ACT Series



HARRIS HIGH-RELIABILITY LEVEL 3A 54AC/ACT ICs (SCREENED TO METHOD 5004 OF MIL-STD-883)

Transistor Count Per Device

DEVICE TYPE	TRANSISTORS
CD54AC00F3A	40
CD54AC02F3A	64
CD54AC04F3A	60
CD54AC05F3A	54
CD54AC08F3A	56
CD54AC32F3A	56
CD54AC74F3A	116
CD54AC109F3A	144
CD54AC112F3A	140
CD54AC138F3A	192
CD54AC139F3A	124
CD54AC153F3A	144
CD54AC157F3A	100
CD54AC161F3A	304
CD54AC163F3A	304
CD54AC164F3A	184
CD54AC191F3A	351
CD54AC193F3A	382
CD54AC240F3A	136
CD54AC244F3A	152
CD54AC245F3A	368
CD54AC257F3A	162
CD54AC273F3A	258
CD54AC280F3A	180
CD54AC283F3A	226

DEVICE TYPE	TRANSISTORS
CD54AC299F3A	627
CD54AC373F3A	142
CD54AC374F3A	312
CD54AC534F3A	296
CD54AC541F3A	168
CD54AC573F3A	142
CD54AC574F3A	312
CD54ACT00F3A	72
CD54ACT02F3A	64
CD54ACT04F3A	66
CD54ACT05F3A	60
CD54ACT08F3A	64
CD54ACT20F3A	48
CD54ACT32F3A	64
CD54ACT74F3A	116
CD54ACT86F3A	112
CD54ACT109F3A	152
CD54ACT112F3A	152
CD54ACT138F3A	196
CD54ACT139F3A	140
CD54ACT151F3A	208
CD54ACT153F3A	144
CD54ACT161F3A	316
CD54ACT163F3A	316
CD54ACT164F3A	190

DEVICE TYPE	TRANSISTORS
CD54ACT174F3A	232
CD54ACT191F3A	363
CD54ACT193F3A	391
CD54ACT240F3A	136
CD54ACT241F3A	150
CD54ACT244F3A	152
CD54ACT245F3A	420
CD54ACT253F3A	170
CD54ACT257F3A	170
CD54ACT273F3A	268
CD54ACT280F3A	189
CD54ACT283F3A	226
CD54ACT299F3A	663
CD54ACT323F3A	661
CD54ACT373F3A	190
CD54ACT374F3A	314
CD54ACT533F3A	206
CD54ACT534F3A	298
CD54ACT540F3A	198
CD54ACT541F3A	182
CD54ACT573F3A	190
CD54ACT574F3A	314
CD54ACT623F3A	420

Advanced CMOS Logic ICs - AC/ACT Series‡

Absolute Maximum Ratings

Power Dissipation Per Package, P _D Package F
T _A = -55°C to +100°C
T _A = +100°C to +125°C Derate Linearly at 8mW/°C to 300mW
Operating Temperature Range, T _A 55°C to +125°C
Storage Temperature, T _{STG} 65°C to +150°C
Lead Temperature (During Soldering)
At Distance 1/16in. ± 1/32in. (1.59mm ± 0.79mm)
From Case For 10s Max +265°C
Unit Inserted Into a PC Board Min thickness 1/16in., (1.59mm)
With Solder Contacting Lead Tips Only+300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

Supply Voltage Range, V _{CC} (Note 1)	Operating Temperature, T _A
For T _A = Full Package Temperature Range	Input Rise and Fall Slew Rate, dt/dv
AC Types1.5V to 5.5V	1.5V to 3V (AC Types) 50ns/V Max
ACT Types	3.6V to 5.5V (AC Types) 20ns/V Max
DC Input or Output Voltage, V _I , V _O 0 to V _{CC}	4.5V to 5.5V (AC Types)

Standard DC Electrical Specifications - CD54AC Series

Non-standard DC Electrical Specifications are included in the individual data sheets.

		TES'			T _A = -	-25°C	T _A = -5 +12	5°C TO 5°C	
PARAMETERS	SYMBOL	V _I (V)	I _O (mA)	V _{CC} (V)	MIN	MAX	MIN	MAX	UNITS
High Level Input Voltage	V _{IH}			1.5	1.2	-	1.2	-	V
				3	2.1	-	2.1	-	V
				4.5	3.15 (Note 2)	-	3.15 (Note 2)	-	V
				5.5	3.85	-	3.85	-	V
Low Level Input Voltage	V _{IL}			1.5	-	0.3	-	0.3	V
				3	-	0.9	-	0.9	V
				4.5	-	1.35 (Note 2)	-	1.35 (Note 2)	V
				5.5	-	1.65	-	1.65	V
High Level Output Voltage	V _{OH}	V _{IH} or V _{IL}	-0.05	1.5	1.4	-	1.4	-	V
		(Notes 3, 4)	-0.05	3	2.9	-	2.9	-	٧
			-0.05	4.5	4.4	-	4.4	- 1	V
			-4	3	2.58	-	2.4	-	V
			-24	4.5	3.94 (Note 2)	-	3.7 (Note 2)	-	٧
			-50	5.5	-	-	3.85	- 1	V
Low Level Output Voltage	V _{OL}	V _{IH} or V _{IL}	0.05	1.5	-	0.1	-	0.1	V
		(Notes 3, 4)	0.05	3	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	٧
			12	3	-	0.36	-	0.5	V
			24	4.5	-	0.36 (Note 2)	-	0.5 (Note 2)	V
			50	5.5	-	-	-	1.65	V
Input Leakage Current	l ₁	V _{CC} or GND		5.5	-	±0.1 (Note 2)	-	±1.0 (Note 2)	μА
Three-State Leakage Current (Note 5)	loz	V_{IH} or V_{IL} $V_{O} = V_{CC}$ or GND		5.5	-	±0.5 (Note 2)	-	±10 (Note 2)	μА

[‡] For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX. See Section 8, "How to use AnswerFAX", in this selection guide.

Advanced CMOS Logic ICs - AC/ACT Series‡

Standard DC Electrical Specifications - CD54AC Series (Continued)

Non-standard DC Electrical Specifications are included in the individual data sheets.

			TES' CONDIT	-		T _A = 4	-25°C	T _A = -55 +12	5°C TO 5°C	
PARAMETERS		SYMBOL	V _I (V)	I _O (mA)	V _{CC} (V)	MIN	MAX	MIN	MAX	UNITS
Quiescent Supply Current (Note 6)	MSI	Icc	V _{CC} or GND	0	5.5	-	8 (Note 2)	-	160 (Note 2)	μА
	SSI/FF			0	5.5	-	4 (Note 2)	-	80 (Note 2)	μА

NOTES:

- 1. Unless otherwise specified, all voltages are referenced to ground.
- 2. These limits are tested 100%.
- 3. Test one output at a time for a 1s maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
- 4. Test verifies a minimum transmission-line-drive capability of 75Ω for 54AC/ACT Series.
- 5. Individual data sheets will indicate where applicable.
- 6. Individual data sheets will indicate complexity.

Standard DC Electrical Specifications - CD54ACT Series

Non-standard DC electrical specifications are included in the individual data sheets.

		TEST CONDITIO	NS		T _A = +	-25°C	T _A = -55 +12		
PARAMETERS	SYMBOL	V _I (V)	l _O (mA)	V _{CC} (V)	MIN	MAX	MIN	MAX	UNITS
High Level Input Voltage	V _{IH}			4.5 to 5.5	2 (Note 1)	-	2 (Note 1)	-	V
Low Level Input Voltage	V _{IL}			4.5 to 5.5	-	0.8 (Note 1)	-	0.8 (Note 1)	V
High Level Output Voltage	V _{OH}	V _{IH} or V _{IL}	-0.05	4.5	4.4	-	4.4	-	V
		(Note 2 and Note 3)	-24	4.5	3.94 (Note 1)	-	3.7 (Note 2)	-	V
			-50	5.5	-	-	3.85	-	V
Low Level Output Voltage	V _{OL}	V _{IL} or V _{IH}	0.05	4.5	-	0.1	-	0.1	V
		(Note 2 and Note 3)	24	4.5	-	0.36 (Note 1)	-	0.5 (Note 1)	٧
			50	5.5	-	-	-	1.65	V
Input Leakage Current	I _I	V _{CC} or GND		5.5	-	±0.1 (Note 1)	-	±1.0 (Note 1)	μА
Three-State Leakage Current (Note 4)	l _{oz}	V_{IH} or V_{IL} $V_{O} = V_{CC}$ or GND		5.5	-	±0.5 (Note 1)	-	±10 (Note 1)	μА
Quiescent Supply MSI Current (Note 5)	Icc	V _{CC} or GND	0	5.5	-	8 (Note 1)	-	160 (Note 1)	μА
SSI/FF				5.5	-	4 (Note 1)	-	80 (Note 1)	μА
Additional Supply Current per Input Pin, TTL Inputs High, 1 Unit Load	Δl _{CC}	V _{CC} - 2.1		4.5 to 5.5	-	2.4	-	3	mA

NOTES:

- 1. These limits are tested 100%.
- 2. Test one output at a time for a 1s maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
- 3. Test verifies a minimum transmission-line-drive capability of 75 Ω for CD54AC/ACT Series.
- 4. Individual data sheet will indicate open-drain types.
- 5. Individual data sheet will indicate complexity.

Prerequisite for Switching - AC/ACT

Refer to the commercial data sheet for the device type of interest. See Section 8, "How to Use AnswerFAX", in this selection guide.

6-22

[‡] For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX. See Section 8, "How to use AnswerFAX", in this selection guide.

Features

The Harris High-Reliability CD4000B Series of high-voltage CMOS integrated circuits consists of a broad range of SSI, MSI-1, and MSI-2 (LSI) functions from simple gates to complex counters, registers, and arithmetic circuits. Specific design features for CMOS devices and the performance advantages of CMOS technology - low power consumption, high noise immunity, high speed, high fanout TTL and DTL logic compatibility, excellent temperature stability, and fully protected inputs and outputs - provide the logic system designer with a capability to achieve outstanding performance, high reliability and simplified circuitry in a wide variety of equipment designs.

- 100% Tested for Quiescent Current at 20V
- Maximum Input Current (Leakage of 1μA at 18V Over Full Package-Temperature Range; 100nA at 18V at +25°C
- · Standardized Symmetrical Output Characteristics
- · 5V, 10V, and 15V Parametric Ratings
- Noise Margin (Over Full Package-Temperature Range)
 - 1V at V_{DD} = 5V
 - 2V at V_{DD} = 10V
 - 2.5V at V_{DD} = 15V
- Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Buffered vs Unbuffered Gates

The new industry standard establishes a suffix "UB" for CMOS products that meet all B-Series specifications except that the logical outputs of the devices are not buffered and the $V_{\rm IL}$ and $V_{\rm IH}$ specifications are 20% and 80% of $V_{\rm DD}$, respectively. See Application Note AN6558, "Understanding Buffered and Unbuffered CMOS Characteristics". See Section 8, "How to Use AnswerFAX", in this selection guide. The suffix "B" defines high voltage buffered output devices in which the output "on" impedance is independent of any and all valid input logic conditions, both preceding and present.

Both buffered "B" and unbuffered "UB" versions of the popular NOR and NAND gates are supplied to make available to designers the advantages of both. The following table briefly compares the features of the two versions.

CHARACTERISTIC	BUFFERED VERSION "B"	UNBUFFERED VERSION "UB"
Propagation Delay (Speed)	Moderate	Fast
Noise Immunity/Margin	Excellent	Good
Output Impedance and Output Transition Time	Constant	Variable
AC Gain	High	Low
Output Oscillation for Slow Inputs	Yes	No
Input Capacitance	Low	High

Compliance to MIL-STD-883

Harris CD4000 Series parts are in full compliance with Paragraph 1.2.1 of MIL-STD-883. Product is provided to meet the requirements of Class B.

SMD or DESC drawing parts are in full compliance with Paragraph 1.2.1 of MIL-STD-883 and meet the SMD or DESC drawings.

Suffix 3A meets Class B requirements. Electrical tests are performed to parameters described in the Electrical Specifications.

Harris also provides CD4000 Series parts that meet the requirements of MIL-STD-883, Paragraph 1.2.2. This family of parts has the following designation.

Suffix 3 meets most of the requirements of a Class B part as described in details presented in the Lot Screening and Product Flow tables.

JAN M38535 CMOS ICs

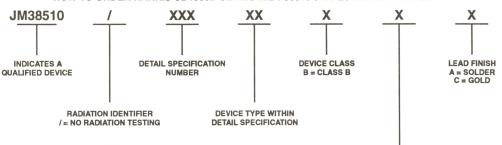
The Harris High-Reliability product line also provides devices that are manufactured and tested in accordance with the MIL-I-38535 (detailed and general) specification, which includes methods and procedures of the Military Standard MIL-STD-883.

SCREENING LEVELS FOR STANDARD HARRIS HIGH-RELIABILITY CD4000B-SERIES INTEGRATED CIRCUITS

S	CREENING LEVELS	APPLICATION	DESCRIPTION	PACKAGE OPTIONS
ЗА	Class B (Full Compliance)	Mil. and Ind. For example, in Airborne	For devices intended for use where maintenance and	F
3	Class B, Modified	Electronics	replacement can be performed but are difficult and expensive.	D, K

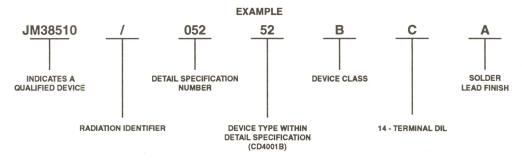
Product Ordering Information

HOW TO ORDER HARRIS CD4000B SERIES MIL-I-38510 JAN-QUALIFIED PRODUCT



PACKAGE OUTLINE

LETTER = TERMINALS	PACKAGE	CASE OUTLINE	CONFIGURATION
C = 14	DIL	D-1	1
E = 16	DIL	D-2	1



Branding: JAN products are single branded with the MIL-I-38510 nomenclature.

Product Ordering Information (Continued)

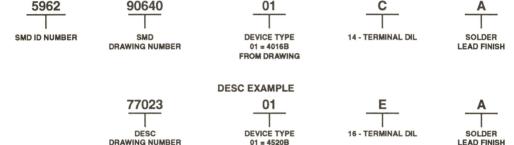
HOW TO ORDER SMD AND DESC DRAWING PRODUCT



PACKAGE OUTLINE

LETTER = TERMINALS	CASE OUTLINE	CONFIGURATION	
C = 14	D-1	1	
E = 16	D-2	1	
J = 24	D-3	1	





Branding: SMD/DESC products are double branded with both the Harris nomenclature and SMD/DESC nomenclature.

FROM DRAWING

HOW TO ORDER HARRIS STANDARD CD4000 SERIES /883 SCREENED PRODUCT



 PACKAGE DESIGNATOR
 RELIABILITY SCREENING LEVEL

 D = DUAL-IN-LINE METAL SEAL CERAMIC
 3A = CLASS B, MIL-STD-883

 K = FLAT PACK
 3 = CLASS B, MODIFIED

 F = DUAL-IN-LINE FRIT SEAL CERAMIC
 3 = CLASS B, MODIFIED

Description of Data Supplied

JAN or Class B Product

- · Processing and Screening Compliance C of C
- · Group A Attribute Summary
- · Group B Attribute Summary
- Groups C and D Attribute Summary when tests are performed on product being supplied; or Date of Performance when tests are covered by another type from the same microcircuit group.

Suffix 3A Harris /883 Full Compliant

- Processing and Screening Compliance C of C
- · Group A Attribute Summary
- Group B Attribute Summary
- Group C and D Attribute Summary Available Per Request at Added Cost

3

Suffix 3 Harris /883 Non Compliant

- · Processing and Screening Compliance C of C
- · Group A Attribute Summary

Product Number Selection Guide

GENERIC PART NUMBER	TYPE NUMBER	CIRCUIT FUNCTION	PACKAGE DESIGNATOR	STANDARD SCREENING LEVELS	NUMBER OF PINS
4000A	CD4000A	Dual 3-Input NOR Gate Plus Inverter	F	В	14
4000B	CD4000B	Dual 3-Input NOR Gate Plus Inverter	D	3	14
4000UB	CD4000UB	Dual 3-Input NOR Gate Plus Inverter	D	3	14
4001A	CD4001A	Quad 2-Input NOR Gate	F	В	14
			D, K	3	1
4001B	CD4001B	Quad 2-Input NOR Gate	F	В	14
			F	ЗА	1
			D, K	3	1
4001UB	CD4001UB	Quad 2-Input NOR Gate	F	В	14
			D	3	1
4002A	CD4002A	Dual 4-Input NOR Gate	D	3	14
4002B	CD4002B	Dual 4-Input NOR Gate	F	В	14
			F	3A	1
			D, K	3	1
4002UB	CD4002UB	Dual 4-Input NOR Gate	F	3A	14
			D, K	3	1
4006A	CD4006A	18-Stage Static Shift Register	D	3	14
4006B	CD4006B	18-Stage Static Shift Register	F	3A	14
		,	D	3	
4007A	CD4007A	Dual Complementary Pair Plus Inverter	F	В	14
			D	3	1
4007UB	CO4007UB	Dual Complementary Pair Plus Inverter	F	3A	14
			D	3	1
4008B	CD4008B	4-Bit Full Adder with Parallel Carry-Out	F	3A	16
			D	3	1
4009UB	CD4009UB	Hex Buffer/Converter (Inverting)	F	ЗА	16
			D, K	3	1
4010B	CD4010B	Hex Buffer/Converter (Non-Inverting)	F	ЗА	16
			D, K	3	1
4011A	CD4011A	Quad 2-Input NAND Gate	F	В	14
			D, K	3	1
4011B	CD4011B	Quad 2-Input NAND Gate	F	В	14
			F	3A	1
			D, K	3	7
4011UB	CD4011UB	Quad 2-Input NAND Gate	F	3A	14
			D	3	1
4012A	CD4012A	Dual 4-Input NAND Gate	D	3	14

GENERIC PART NUMBER	TYPE NUMBER	CIRCUIT FUNCTION	PACKAGE DESIGNATOR	STANDARD SCREENING LEVELS	NUMBER OF PINS
4012B	CD4012B	Dual 4-Input NAND Gate	F	В	14
			F	3A	1
			D	3	
4013A	CD4013A	Dual "D" Flip-Flop with Set/Reset Capability	F	В	14
4013B	CD4013B	Dual "D" Flip-Flop with Set/Reset Capability	F	В	14
			F	3A	1
			D, K	3	
4014A	CD4014A	8-Stage Static Shift Register	D	3	16
4014B	CD4014B	8-Stage Static Shift Register	F	3A	16
			D	- 3	1
4015A	CD4015A	Dual 4-Stage Static Shift Register	D	3	16
4015B	CD4015B	Dual 4-Stage Static Shift Register	F	3A	16
			D, K	3	
4016A	CD4016A	Quad Bilateral Switch	D	3	14
4016B CD4016B	CD4016B	CD4016B Quad Bilateral Switch	F	3A	14
			D, K	3	
4017A	CD4017A	Decade Counter/Divider	F	В	16
			D	3	1
4017B	CD4017B	CD4017B Decade Counter/Divider	F	В	16
			F	3A	-
			D	3	
4018A	CD4018A	Presettable Divide-By "N" Counter	D	3	16
4018B	CD4018B	4018B Presettable Divide-By "N" Counter	F	В	16
			F	3A	1
			D, K	3	1
4019A	CD4019A	Quad AND/OR Select Gate	F	В	16
			D	3	1
4019B	CD4019B	Quad AND/OR Select Gate	F	В	16
			, F	ЗА	
			D, K	3	
4020A	CD4020A	14-Stage Binary Ripple Counter	F	В	16
			D, K	3	
4020B	CD4020B	14-Stage Binary Ripple Counter	F	В	16
			F	3A	
			D	3	
4021A	CD4021A	8-Stage Static Shift Register	D, K	3	16
4021B	CD4021B	8-Stage Static Shift Register	F	В	16
			F	3A	
			D, K	3]

GENERIC PART NUMBER	TYPE NUMBER	CIRCUIT FUNCTION	PACKAGE DESIGNATOR	STANDARD SCREENING LEVELS	NUMBE OF PINS
4022A	CD4022A	Divide-by-8 Counter/Divider	D	3	16
4022B	CD4022B	Divide-by-8 Counter/Divider	F	3A	16
			D	3	1
4023A	CD4023A	Triple 3-Input NAND Gate	F	В	14
			D, K	3	1
4023B	CD4023B	Triple 3-Input NAND Gate	F	В	14
			F	3A	1
			D, K	3	1
4023UB	CD4023UB	Triple 3-Input NAND Gate	D	3	14
4024A	CD4024A	7-Stage Binary Ripple Counter	F	В	14
			D, K	3	1
4024B	CD4024B	7-Stage Binary Ripple Counter	F	В	14
			F	3A	1
			D, K	3	1
4025A	CD4025A	Triple 3-Input NOR Gate	F	В	14
			D	3	1
4025B	CD4025B	Triple 3-Input NOR Gate	F	В	14
			F	3A	1
			D	3	1
4025UB	CD4025UB	Triple 3-Input NOR Gate	D	3	14
4027A	CD4027A	Dual "J-K" Flip-Flop with Set/Reset Capability	F	В	16
			D, K	3	1
4027B	CD4027B	Dual "J-K" Flip-Flop with Set/Reset Capability	F	В	16
			F	3A	1
			D, K	3	
4028A	CD4028A	BCD-to-Decimal Decoder	D	3	16
4028B	CD4028B	BCD-to-Decimal Decoder	F	3A	16
			D, K	3	
4029A	CO4029A	Presettable Up/Down Counter	D	3	16
4029B	CD4029B	Presettable Up/Down Counter	F	3A	16
			D, K	3	
4030A	CD4030A	Quad Exclusive-OR Gate	D	3	14
4030B	CD4030B	Quad Exclusive-OR Gate	F	В	14
			F	3A	
			D, K	3	\dashv
4031A	CD4031A	64-Stage Static Shift Register	D	3	16
4031B	CD4031B	64-Stage Static Shift Register	F	3A	16
			D, K	3	

GENERIC PART TYPE NUMBER NUMBER CIRCUIT FUNCTION		CIRCUIT FUNCTION	PACKAGE DESIGNATOR	STANDARD SCREENING LEVELS	NUMBER OF PINS
4033B	CD4033B	Decade Counter/Divider	D	3	16
4034B	CD4034B	8-Stage Static Shift Register	F	3A	24
			D	3	1
4035B	CD4035B	4-Stage Parallel-In/Parallel-Out Shift Register	F	ЗА	24
			D, K	3	1
4040A	CD4040A	12-Stage Binary Ripple Counter	D, K	3	16
4040B	CD4040B	12-Stage Binary Ripple Counter	F	3A	16
			D	3	1
4041A	CD4041A	Quad True/Complement Butter	D	3	14
4041UB	CD4041UB	Quad True/Complement Buffer	F	3A	14
			D, K	3	
4042A	CD4042A	Quad Clocked "D" Latch	D, K	3	16
4042B	CD4042B Quad Clocked "D" Latch	F	3A	16	
			D, K	3	1
4043A	CD4043A	Quad NOR R/S Latch (Three-State Outputs)	D	3	16
4043B	CD4043B Quad NOR R/S Latch (Three-State Outputs)	F	3A	16	
			D	3	
4044A	CD4044A	Quad NAND R/S Latch (Three-State Outputs)	D	3	16
4044B	CO4044B	4044B Quad NAND R/S Latch (Three-State Outputs) F	3A	16	
			D	3	
4046A	CD4046A	Micropower Phase-Locked Loop	D	3	16
4046B	CD4046B	Micropower Phase-Locked Loop	F	3A	16
			D, K	3	
4047B	CD4047B	Monostable/Astable Multivibrator	F	ЗА	14
			D	3	
4048A	CD4048A	Multifunctional Expandable 8-Input Gate (Three-State Output)	D	3	16
4048B	CD4048B	Multifunctional Expandable 8-Input Gate	F	3A	16
		(Three-State Outputs)	D	3	
4049A	CD4049A	Hex Buffer/Converter (Inverting)	F	В	16
			D	3	
4049UB	CD4049UB	Hex Buffer/Converter (Inverting)	F	В	16
			F	3A	
			D, K	3	
4050A	CD4050A	Hex Buffer/Converter (Non-Inverting)	F	В	16
			D	3	
4050B	CD4050B	Hex Buffer/Converter (Non-Inverting)	F	В	16
			F	3A	
			D, K	3	

GENERIC PART TYPE NUMBER NUMBER		PART TYPE		STANDARD SCREENING LEVELS	NUMBER OF PINS
4051B	CD4051B	8-Channel Analog Multiplexer/Demultiplexer	F	ЗА	16
			D, K	3	1
4052B	CD4052B	4-Channel Analog Multiplexer/Demultiplexer	F	ЗА	16
			D, K	3	1
4053B	CD4053B	Analog Multiplexers/Demultiplexers	F	3A	16
		Triple 2-Channel	D	3	
4054B	CD4054B	4-Segment Display Driver	F	ЗА	16
4056B	CD4056B	BCD-to-7-Segment Decoder/Driver with Strobed-Latch Function	F	3A	16
4059A	CD4059A	Programmable Divide-by-"N" Counter	D	3	24
4060A	CD4060A	14-Stage Binary Ripple Counter/Divider and Oscillator	D	3	16
4060B	CD4060B		F	3A	16
		Oscillator	D	3	1
4063B	CD4063B 4-Bit Magnitude Comparator	F	ЗА	16	
			D, K	3	1
4066B	CD4066B	Quad Bilateral Switch	F	В	14
			F	ЗА	
			D, K	3	1
4067B	CD4067B	16-Channel Analog Multiplexers/Demultiplexers	F	ЗА	24
			D	3	
4068B	CD4068B	8-Input NAND/AND Gate	F	3A	14
			D	3	
4069UB	CD4069UB	Hex Inverter	F	В	14
			F	ЗА]
			D	3	
4070B	CD4070B	Quad Exclusive-OR Gate	F	В	14
			F	3A]
			D	3	
4071B	CD4071B	Quad 2-Input OR Gate	F	В	14
			F	3A	
			D, K	3	
4072B	CD4072B	Dual 4-Input OR Gate	F	3A	14
			D	3	
4073B	CD4073B	Triple 3-Input AND Gate	F	В	14
			F	3A	
			D	3]

GENERIC PART NUMBER			PACKAGE DESIGNATOR	STANDARD SCREENING LEVELS	NUMBER OF PINS
4075B	CD4075B	Triple 3-Input OR Gate	F	В	14
			F	3A	
			D, K	3	
4076B	CD4076B	4-Bit "D" Flip-Flop (Three-State Outputs)	F	3A	16
			D	3	
4077B	CD4077B	Quad Exclusive-NOR Gate	F	3A	14
			D	3	
4078B	CD4078B	8-Bit NOT/OR Gate	F	3A	14
			D	3	
4081B	CD4081B	Quad 2-Input AND Gate	F	В	14
			F	ЗА	
			D, K	3	
4082B	CD4082B	Dual 4-Input AND Gate	F	В	14
			F	ЗА	
			D	3	
4085B	CD4085B	Dual 2-Wide, 2-Input AND/OR/INVERT (AOI)	F	3A	14
		Gate	D	3	
4086B	CD4086B	Expandable 4-Wide, 2-Input AND/OR/INVERT	F	3A	14
		(AOI) Gate	D	3	
4089B	CD4089B	D4089B Binary Rate Multiplier	F	3A	16
			D	3	
4093B	CD4093B	Quad 2-Input NAND Schmitt Trigger	F	3A	14
			D	3	
4094B	CD4094B	8-Stage Shift-and-Store Bus Register	F	ЗА	16
			D	3	
4095B	CD4095B	Gated "J-K" Flip-Flop (Non-Inverting)	F	3A	14
			D	3	
4096B	CD4096B	Gated "J-K" Flip-Flop (Inverting and Non-Inverting)	D	3	14
4097B	CD4097B	8-Channel Analog Multiplexer/Demultiplexer	D	3	24
4098B	CD4098B	Dual Monostable Multivibrator	F	В	16
			F	ЗА	
			D, K	3	
4099B	CD4099B	8-Bit Addressable Latch	F	B 16	
			F	3A	
			D, K	3	
4502B	CD4502B	Strobed Hex Inverter/Buffer	F	В	16
			F	3A	
			D, K	3	

GENERIC PART NUMBER	TYPE NUMBER	CIRCUIT FUNCTION	PACKAGE DESIGNATOR	STANDARD SCREENING LEVELS	NUMBER OF PINS	
4503B	CD4503B	Hex Buffer (Non-Inverting)	F	ЗА	16	
			D	3		
4504B	CD4504B	Hex Voltage-Level Shifter for TTL-to-CMOS CMOS-to-CMOS Operation	F	3A	16	
4508B	CD4508B	Dual 4-Bit Latch	F	3A	24	
			D, K	3		
4510B	CD4510B	Presettable 4-Bit BCD Up/Down Counter	F	3A	16	
			D	3		
4511B	CD4511B	BCD-to-7-Segment Latch Decoder/Driver	F	3A	16	
			D, K	3		
4512B	CD4512B	8-Channel Data Selector (Three-State Output)	F	ЗА	16	
			D	3	1	
4514B	CD4514B	4-Bit Latch/4-to-16 Line Decoder (Outputs Low)	F	3A	24	
			D	3	1	
4515B	CD4515B	4-Bit Latch/4-to-16 Line Decoder (Outputs Low)	F	ЗА	24	
			D	3	1	
4516B	CD4516B	Presettable 4-Bit Binary Up/Down Counter	F	ЗА	16	
			D	3	1	
4517B	CD4517B	Dual 64-Bit Shift Register	F	3A	16	
			D	3	1	
4518B	CD4518B	Dual BCD Up Counter	F	ЗА	16	
			D	3	1	
4520B	CD4520B	Dual Binary Up Counter	F	ЗА	16	
			D	3	1	
4527B	CD4527B	BCD Rate Multiplier	D	3	16	
4532B	CD4532B	8-Input Priority Encoder	F	ЗА	16	
			D	3		
4536B	CD4536B	Programmable Timer	F	ЗА	16	
			D	3	1	
4541B	CD4541B	CMOS Programmable Timer	F	ЗА	14	
4555B	CD4555B	Dual 1 of 4 Decoder/Demultiplexer (Outputs High)	F	ЗА	16	
4556B	CD4556B	Dual Binary to 1 of 4 Decoder/Demultiplexers	F	ЗА	16	
		(Outputs Low)	D	3	1	
4585B	CD4585B	4-Bit Magnitude Comparator	F	3A	16	
4724B	CD4724B	8-Bit Addressable Latch	F	3A	16	
14538B	CD14538B	Dual Precision Monostable Multivibrator	F	3A	16	
40100B	CD40100B	9-Bit Parity Generator/Checker	D	3	16	

GENERIC PART NUMBER	PART TYPE NUMBER NUMBER CIRCUIT FUNCTION		PACKAGE DESIGNATOR	STANDARD SCREENING LEVELS	NUMBER OF PINS	
40101B	CD40101B	9-Bit Parity Generator/Checker	F	ЗА	14	
			D	3	7	
40102B	CD40102B	Presettable 2-Decade BCD Down Counter	D	3	16	
40103B	CD40103B	Presettable 8-Bit Binary Down Counter	F	ЗА	16	
			D	3	1	
40104B	CD40104B	4-Bit Bidirectional Universal Shift Register	-Bit Bidirectional Universal Shift Register D		16	
40105B	CD40105B	4-Bit X 16 Word FiFo Buffer Register	F	3A	16	
			D, K	3	1	
40106B	CD40106B	Hex Schmitt Trigger	F	3A	14	
			D, K	3	1	
40107B	CD40107B Dual 2-Input NAND Buffer/Driver		F	ЗА	14	
			D	3	1	
40108B	CD40108B	4 X 4 Multiport Register	D	3	24	
40109B	CD40109B	Quad Low-to-High Voltage Interface	F	ЗА	16	
			D, K	3		
40116	CD40116	CMOS High Speed 8-Bit Directional D CMOS/TTL Interface Level Converter (GP511 is Rad-Hard Version)		3	22	
40160B	CD40160B	Synchronous Programmable 4-Bit Counter F 3A Decade with Asynchronous Clear		3A	16	
40161B	CD40161B	Synchronous Programmable 4-Bit Counter	F	ЗА	16	
,		Binary with Asynchronous Clear	D	3		
40163B	CD40163B	Synchronous Programmable 4-Bit Counter Binary with Synchronous Clear	F	3A	16	
40174B	CD40174B	Hex "D" Type Flip-Flop	F	ЗА	16	
			D	3		
40175B	CD40175B	Quad 'D' Type Flip-Flop	F	ЗА	16	
40192B	CD40192B	CMOS Look-Ahead Carry Generator	F	ЗА	16	
			D	3		
40193B	CD40193B	CMOS Presettable Up/Down Counters	F	3A	16	
		(Dual Clock with Reset)	D	3		
40194B	CD40194B	4-Bit Bidirectional Universal Shift Register	D, K	3	16	
40257B	CD40257B	Quad 2-Line-to-1-Line Data Selector/Multiplexer	F	3A	16	
			D	3		

MIL-I-38535 to Harris Hi-Rel Types Sorted by JAN Type

MIL-I	HARRIS
DESIGNATION	TYPE
JM38510/05001BCA	CD4011AFB
JM38510/05003BCA	CD4023AFB
JM38510/05051BCA	CD4011BFB
JM38510/05052BCA	CD4012BFB
JM38510/05053BCA	CD4023BFB
JM38510/05101BCA	CD4013AFB
JM38510/05102BEA	CD4027AFB
JM38510/05151BCA	CD4013BFB
JM38510/05152BEA	CD4027BFB
JM38510/05201BCA	CD4000AFB
JM38510/05202BCA	CD4001AFB
JM38510/05204BCA	CD4025AFB
JM38510/05252BCA	CD4001BFB
JM38510/05254BCA	CD4025BFB

MIL-I	HARRIS
DESIGNATION	TYPE
JM38510/05301BCA	CD4007AFB
JM38510/05302BEA	CD4019AFB
JM38510/05352BEA	CD4019BFB
JM38510/05353BCA	CD4030BFB
JM38510/05503BEA	CD4049AFB
JM38510/05504BEA	CD4050AFB
JM38510/05553BEA	CD4049UBFB
JM38510/05554BEA	CD4050BFB
JM38510/05601BEA	CD4017AFB
JM38510/05603BEA	CD4020AFB
JM38510/05605BCA	CD4024AFB
JM38510/05651BEA	CD4017BFB
JM38510/05652BEA	CD4018BFB
JM38510/05653BEA	CD4020BFB

MIL-I	HARRIS
DESIGNATION	TYPE
JM38510/05655BCA	CD4024BFB
JM38510/05754BEA	CD4021BFB
JM38510/05852BCA	CD4066BFB
JM38510/17001BCA	CD4081BFB
JM38510/17002BCA	CD4082BFB
JM38510/17003BCA	CD4073BFB
JM38510/17101BCA	CD4071BFB
JM38510/17103BCA	CD4075BFB
JM38510/17203BCA	CD4070BFB
JM38510/17401BCA	CD4069UBFB
JM38510/17403BEA	CD4502BFB
JM38510/17504BEA	CD4098BFB
JM38510/17601BEA	CD4099BFB

SMD or DESC Parts List

SMD OR DESC NUMBER	HARRIS PART NUMBER
7702002EA	CD4502BF3A
7702301EA	CD4520BF3A
7702402CA	CD4081BF3A
7702501EA	CD4094BF3A
7703201JA	CD4515BF3A
7703702EA	CD4585BF3A
7704402CA	CD4078BF3A
7704403CA	CD4002BF3A
7704701EA	CD4555BF3A
7704801EA	CD4556BF3A
7705102CA	CD4073BF3A
7705902CA	CD4082BF3A
7706002CA	CD4072BF3A
8101602EA	CD4029BF3A
8101801EA	CD4053BF3A
8102001CA	CD4047BF3A
5962-9064001CA	CD4016BF3A
5962-9055701EA	CD14538BF3A
7704602CA	CD4093BF3A
7901502EA	CD4052BF3A
8101701EA	CD4035BF3A

NOTE:

Lot Screening Tests

The Total Lot Screening Table indicates the screening performed on JAN B, 3 and 3A devices. 3 and 3A are equivalent to MIL-STD-883 Class B screens to Method 5004. As shown in the Manufacturing and Conformance Testing table, the differences between a 3 and 3A is the lead finish and pellet mounting technique. It should be noted that all CD4XXXB-Series wafers are manufactured at the Harris JAN certified plant in Findlay, Ohio and any JAN type manufactured in the U.S. is completely assembled and tested on our JAN-certified line.

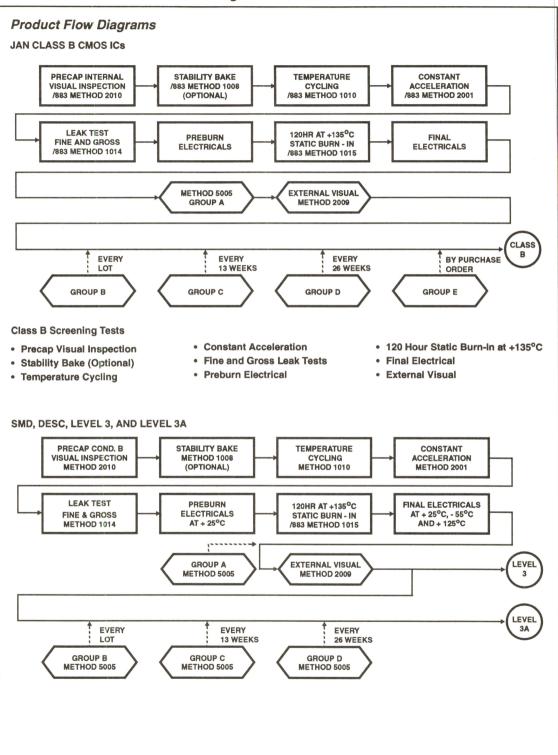
^{1.} Product is dual branded with SMD/DESC and Harris part number.

Total Lot Screening For High-Reliability CD4000B Series ICs

SCREENING TESTS	TEST CONDITIONS	METHOD	PRODUCT JAN B, 3, 3A, AND SMD	NOTES		
Pre-Cap Visual at Assembly	Condition B	2010	х	•		
PRECONDITIONING						
Stabilization Bake (Optional)	Condition C	1008	х	-		
Temperature Cycle	Condition C	1010	х	-		
Centrifuge	Condition E, Y1 Only	2001	х	-		
Fine Leak	Condition B	1014	х	-		
Gross Leak	Condition C	1014	х	-		
TEST AND BURN-IN						
Initial Test		-	Х	1		
Static Burn-In 2 120 Hours	+135°C Inputs at V _{DD} , Outputs Open	1015	х	1, 2, 3, 4		
Final Elec DC +25°C		-	Х	-		
Final Elec DC+125°C		-	Х	•		
Final Elec DC -55°C		-	Х	•		
Final Elec AC +25°C		-	х	-		
FINAL INSPECTION	FINAL INSPECTION					
Quality Conformance Inspection (Group A)		5005	х	-		
100% Visual Inspect		2009	х	-		

NOTES:

- 1. See individual data bulletins for electrical testing of specific types or JAN Slash Sheets as applicable.
- 2. Alternate time/temp regression used per /883 Method 1015.
- 3. PDA for 3 and 3A is 5%, one reburn allowed at 3%.
- 4. PDA's are based on Group A subgroup 1.



Absolute Maximum Ratings	Reliability Information
DC Supply-Voltage Range, V_{DD} (Voltages Referenced to V_{SS} Terminal)0.5V to +20V Input Voltage Range, All Inputs -0.5V to V_{DD} +0.5V DC Input Current, Any One Input. ± 10 mA Operating Temperature Range, T_{A}	Thermal Resistance θ_{JA} θ_{JC} Package Types D and F
Package Types D, F, K	Package Types D, F, K
From Case for 10s Maximum +265°C	T _A = Full Package Temperature Range All Package Types

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

Supply Voltage Range

For T_A = Full Package Temperature Range......3V to 18V

Device Classification for Leakage Current

The table below classifies the levels of device leakage as SSI, MSI-1 and MSI-2. In order to determine the limits which apply to specific device type, consult the Standard DC Electrical Specifications table.

Classification According To Circuit Complexity

GATES/INVERTERS (SSI)		LATCHES/N	LIP-FLOPS/ IULTILEVEL (MSI-1)	co	OMPLEX LOGIC (MS	SI-2)
CD4000B	CD4025B	CD4009UB (Note 1)	CD4085B	CD4006B	CD4056B (Note 1)	CD4541B
CD4000UB	CD4025UB	CD4010B (Note 1)	CD4086B	CD4008B	CD4060B	CD4555B
CD4001B	CD4048B	CD4013B	CD4093B (Note 1)	CD4014B	CD4063B	CD4556B
CD4001UB	CD4066B (Note 1)	CD4019B	CD4095B	CD4015B (Note 1)	CD4067B (Note 1)	CD4585B
CD4002B	CD4068B	CD4027B	CD4096B	CD4017B	CD4076B	CD4724B
CD4002UB	CD4069UB	CD4030B	CD4098B	CD4018B	CD4089B	CD14538B
CD4007UB	CD4071B	CD4041UB (Note 1)	CD4502B (Note 1)	CD4020B	CD4094B	CD40100B
CD4011B	CD4072B	CD4042B	CD4503B (Note 1)	CD4021B	CD4097B (Note 1)	CD40101B
CD4011UB	CD4073B	CD4043B	CD4504B (Note 1)	CD4022B	CD4099B	CD40102B
CD4012B	CD4075B	CD4044B	CD40106B (Note 1)	CD4024B	CD4508B	CD40103B
CD4016B	CD4078B	CD4047B	CD40107B (Note 1)	CD4028B	CD4510B	CD40104B
(Note 1)	CD4081B	CD4049UB (Note 1)	CD40109B (Note 1)	CD4029B	CD4511B (Note 1)	CD40105B
CD4023B	CD4082B	CD4050B (Note 1)	CD40174B	CD4031B (Note 1)	CD4512B	CD40108B
CD4023UB		CD4070B	CD40175B	CD4033B	CD4514B	CD40116 (Note 1)
		CD4077B	CD40257B	CD4034B	CD4515B	CD40160B
				CD4035B	CD4516B	CD40161B
				CD4040B	CD4517B	CD40163B
				CD4046B (Note 1)	CD4518B	CD40192B
				CD4051B (Note 1)	CD4520B	CD40193B
				CD4052B (Note 1)	CD4527B	CD40194B
			-	CD4053B (Note 1)	CD4532B	
				CD4054B (Note 1)	CD4536B	

NOTE:

Indicates type for which, because of design requirements, one or more DC Specifications differ from the standardized data.
These differences are defined in separate DC Electrical Specifications table.

DC Electrical Specifications - Standard "B" Series Devices

For all CD4000B Series Standard Output CMOS Devices. Parameters are 100% Tested Unless Otherwise Specified.

		TES	CONDIT	IONS	-55	5°C	+2	5°C	+12	5°C	
PARAMET	TERS	v _o	V _{IN}	V _{DD}	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
Functional Test (Not	tes 1 and 2)	-	-	-	-	-	-	-	-	-	
Quiescent Device Current I _{DD} See Classification	SSI Types (Note 3)	-	0, 5	5	-	0.25 (Note 2)	-	0.25 (Note 2)	٠.	7.5 (Note 2)	μА
Table		-	0, 10	10		0.5 (Note 2)	-	0.5 (Note 2)	-	15 (Note 2)	μА
		-	0, 15	15	-	1 (Note 2)	-	1 (Note 2)	-	30 (Note 2)	μА
		-	0, 20	20	-	5	-	5	-	150	μА
	MSI-1 (Note 3 and Note 4)	-	0, 5	5		1 (Note 2)	-	1 (Note 2)	-	30 (Note 2)	μА
	14018 47	-	0, 10	10		2 (Note 2)	-	2 (Note 2)	-	60 (Note 2)	μА
		-	0, 15	15	-	4 (Note 2)	-	4 (Note 2)		120 (Note 2)	μА
		-	0, 20	20	-	20	-	20	-	600	μΑ μΑ μΑ μΑ μΑ μΑ μΑ μΑ μΑ μΑ
	MSI-2 (Note 3)	* -	0, 5	5	-	5 (Note 2)	-	5 (Note 2)		150 (Note 2)	μА
		-	0, 10	10		10 (Note 2)	-	10 (Note 2)	-	300 (Note 2)	μА
		-	0, 15	15		20 (Note 2)		20 (Note 2)	-	600 (Note 2)	μА
			0, 20	20	-	100	-	100	-	3000	μА
Output Low Drive Cu	urrent, I _{OL} Min	0.4	0, 5	5	0.64 (Note 2)	-	0.51	-	0.36 (Note 2)	-	mA
		0.5	0, 10	10	1.6 (Note 2)	-	1.3	-	0.9 (Note 2)	-	mA
		1.5	0, 15	15	4.2 (Note 2)		3.4	-	2.4 (Note 2)	-	mA
Output High Drive C	urrent, I _{OH} Min	4.6	0, 5	5	-0.64		-0.51	-	-0.36 (Note 2)	-	mA
		2.5	0, 5	5	-2.0	-	-1.6	-	-1.15 (Note 2)	-	mA
		9.5	0, 10	10	-1.6	-	-1.3	-	-0.9 (Note 2)	-	mA
		13.5	0, 15	15	-4.2	-	-3.4	-	-2.4 (Note 2)	-	mA

DC Electrical Specifications - Standard "B" Series Devices (Continued)

For all CD4000B Series Standard Output CMOS Devices. Parameters are 100% Tested Unless Otherwise Specified.

		TEST	CONDIT	IONS	-55	5°C	+25	5°C	+125°C		
PARAMET	ERS	V _o	V _{IN}	V _{DD}	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
Output Voltage Low-	Level, V _{OL} Max	-	0, 5	5	-	0.05 (Note 2)	-	0.05 (Note 2)	-	0.05 (Note 2)	٧
		-	0, 10	10	-	0.05 (Note 2)	-	0.05 (Note 2)	-	0.05 (Note 2)	٧
		-	0, 15	15	-	0.05	-	0.05	-	0.05	٧
Output Voltage High-Level, V _{OH} Mir		-	0, 5	5	4.95 (Note 2)	-	4.95 (Note 2)	-	4.95	-	٧
		-	0, 10	10	9.95 (Note 2)	-	9.95 (Note 2)	-	9.95	-	٧
		-	0, 15	15	14.95	-	14.95	-	14.95	-	٧
Input Low Voltage	Buffered (B)	4.5	-	5	-	1.5	-	1.5	-	1.5	٧
VII. WAX		9	-	10	-	3 (Note 2)	-	3	-	3	٧
		13.5	-	15	-	4	-	4	-	4	V
	Unbuffered (UB)	4.5	-	5	-	1 (Note 2)	-	1	-	1	٧
		9	-	10	-	2	-	2	-	2	٧
		13.5	-	15		2.5		2.5		2.5	V
Input High Voltage V _{IH} Min	Buffered (B)	0.5, 4.5	-	5	3.5	-	3.5	-	3.5	-	٧
VIH IVIIII		1, 9	-	10	7	-	7	-	7	-	٧
		1.5, 13.5	•	15	11	-	11	-	11	-	٧
	Unbuffered (UB)	0.5, 4.5	-	5	4	-	4	-	4	-	٧
	(05)	1, 9	-	10	8	-	8	-	8	-	٧
		1.5, 13.5	-	15	12.5	-	12.5	-	12.5	-	V
Input Current I _{IN} (Note 3)		-	0, 20	20	-	±0.1	-	±0.1	-	±1	μА
Three-State Output L Current, I _{OUT} (Note 3		0, 20	0, 20	20	-	±0.4	-	±0.4	-	±12	μА

NOTES:

- 1. At +25°C V_{IN} = 0 20V, V_{DD} = 20V; +125°C V_{IN} = 0 -18V, V_{DD} = 18V; and at -55°C V_{IN} = 0 3V, V_{DD} = 3V.
- 2. These parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
- 3. At -55°C, test is performed with V_{DD} of 18V.
- $4. \ \ CD4047B Maximum \ DC \ supply \ voltage \ V_{DD} \ is \ 13V \ for \ radiation \ hardened \ version \ of \ this \ type \ when \ operating \ with \ RC \ network.$
- 5. For applicable devices only.

Non-Standard DC Electrical Specifications

The table below indicates all devices which are considered to be non-standard. Non-standard devices are types such as bilateral switches (CD4066B), multiplexers (CD4051B), special sink or source currents (CD4049UB, CD4050B) and open drain buffer/drivers (CD40107B) which exhibit non-

standard outputs or special parameters. This table shows the 100% electrical tests that are performed on these specialized devices. These tests take the place of corresponding parameters in the Standard Electrical Specifications table. For the types listed with $R_{\rm ON}$ tests, drive current and output voltage tests should be deleted from the Standard Electrical Specifications table.

Non-Standard DC Electrical Specifications "B" Series Devices

	TES	ST CONDITI	ONS	-55°C	+25	5°C	+125°C	
PARAMETERS	v _o	V _{IN}	V _{DD}	MIN/ MAX	MIN	мах	MIN/ MAX	UNITS
CD4009UB, CD4010B		Constitution of the Edition of the Constitution of the Constitutio			200000000000000000000000000000000000000			
Output Low Drive Current, I _{OL} Min	0.4	0,5	4.5	3.2	2.6	-	1.8	mA
(Note 2)	0.4	0, 5	5	3.75	3 (Note 1)	-	2.1	mA
	0.5	0, 10	10	10.0	8 (Note 1)	-	5.6	mA
	1.5	0, 15	15	30.0	24 (Note 1)	-	16.0	mA
Output High Drive Current, I _{OH} Min (Note 2)	4.6	0, 5	5	-0.25	-0.2 (Note 1)	-	-0.15	mA
	2.5	0, 5	5	-1.0	-0.8 (Note 1)	-	-0.58	mA
	9.5	0, 10	10	-0.55	-0.45 (Note 1)	-	-0.33	mA
	13.5	0, 15	15	-1.65	-1.5 (Note 1)	-	-1.1	mA
CD4016B								
Control Input Voltage Low, V _{IL} Max (Note 2)	$V_{IS} = V_{SS}$, $V_{IS} = V_{DD}$,	$V_{OS} = V_{SS}$	5	0.9 (Note 1)	-	0.7 (Note 1)	0.4 (Note 1)	٧
	II _{IS} I < 10μΑ		10	0.9	-	0.7	0.4	V
			15	0.9 (Note 1)	-	0.7 (Note 1)	0.4 (Note 1)	V
Control Input Voltage High, V _{IH} Min (Note 2)		-	5	3.5 (Note 1)	3.5 (Note 1)	-	3.5 (Note 1)	٧
			10	7.0	7.0	-	7.0	V
			15	11.0 (Note 1)	11.0 (Note 1)	-	11.0 (Note 1)	V
On-State Resistance, R _{ON} Max R _L = 10K Returned to V _{DD} - V _{SS} /2	$V_{IS} = V_{DD} \circ V_{IS} = 4.75 \circ V_{IS}$	or 5.75	10	600 (Note 1)	-	660 (Note 1)	960 (Note 1)	Ω
(Note 2)	$V_{IS} = V_{DD} \text{ o}$ $V_{IS} = 7.25 \text{ o}$	r V _{SS} or 7.75	10	1870 (Note 1)	-	2000 (Note 1)	2600 (Note 1)	Ω
			15	360 (Note 1)	-	400 (Note 1)	600 (Note 1)	Ω
			15	775 (Note 1)	•	850 (Note 1)	1230 (Note 1)	Ω

Non-Standard DC Electrical Specifications "B" Series Devices (Continued)

	TE	ST CONDITION	ONS	-55°C	+2	5°C	+125°C	
PARAMETERS	v _o	V _{IN}	V _{DD}	MIN/ MAX	MIN	MAX	MIN/ MAX	UNITS
CD4031B								
Output Low Drive Current, I _{OL} Min Q	0.4	0, 5	5	2.56	2.04 (Note 1)	-	1.44	mA
(Note 2)	0.5	0, 10	10	6.4	5.2 (Note 1)	-	3.6	mA
	1.5	0, 15	15	16.8	13.6 (Note 1)	-	9.6	mA
Q, Q´, C _{LD} (Note 2)	0.4	0, 5	5	0.64	0.51 (Note 1)	-	0.36	mA
(1002)	0.5	0, 10	10	1.6	1.3 (Note 1)	-	0.9	mA
	1.5	0, 15	15	4.2	3.4 (Note 1)	-	2.4	mA
Output High Drive Current, I _{OH} Min Q, Q, Q', C _{LD} (Note 2)	4.6	0, 5	5	-0.64	-0.51 (Note 1)	-	-0.36	mA
	2.5	0, 5	5	-2.0	-1.6 (Note 1)	-	-1.15	mA
	9.5	0, 10	10	-1.6	-1.3 (Note 1)	-	-0.9	mA
	13.5	0, 15	15	-4.2	-3.4 (Note 1)	-	-2.4	mA
CD4041UB								
Output Low Drive Current, I _{OL} Min (Note 2)	0.4	0, 5	5	2.1	1.6 (Note 1)	-	1.2	mA
	0.5	0, 10	10	6.25	5 (Note 1)	-	3.5	mA
	1.5	0, 15	15	24	19 (Note 1)	-	13	mA
Output High Drive Current, I _{OH} Min (Note 2)	4.6	0, 5	5	-2.1	-1.6 (Note 1)	-	-1.2	mA
	2.5	0, 5	5	-8.4	-6.4 (Note 1)	-	-4.6	mA
	9.5	0, 10	10	-6.25	-5 (Note 1)	-	-3.5	mA
	13.5	0, 15	15	-24	-19 (Note 1)	-	-13	mA
CD4046B				-				
Zener Diode Voltage (V _Z) (Note 3)		I _Z = 50μA		-	4.45 (Note 1)	6.5 (Note 1)	-	٧
Quiescent Leakage, Phase Comparator	-	0, 5	5	0.2		0.2	-	mA
Pin 14 Open, Pin 5 = V _{DD} (Note 3)	-	0, 10	10	1.0		1.0	-	mA
	-	0, 15	15	1.5		1.5	-	mA
		0, 20	20	4.0 (Note 1)	-	4.0 (Note 1)	-	mA

Non-Standard DC Electrical Specifications "B" Series Devices (Continued)

	TES	ST CONDITIO	ONS	-55°C	+2	5°C	+125°C	
PARAMETERS	v _o	V _{IN}	V _{DD}	MIN/ MAX	MIN	MAX	MIN/ MAX	UNITS
CD4046B (Continued)								
Quiescent Leakage, Phase Comparator		0, 5	5	20	-	20	-	μА
Pin 14 = V_{SS} or V_{DD} , Pin 5 = V_{DD} (Note 3)	-	0, 10	10	40	-	40	-	μА
	-	0, 15	15	80	-	80	-	μА
	-	0, 20	20	160 (Note 1)	-	160 (Note 1)	-	μА
CD4049UB, CD4050B								
Output Low Drive Current, I _{OL} Min (Note 2)	0.4	0,5	4.5	3.3	2.6 (Note 1)	-	1.8	mA
	0.4	0, 5	5	4.0	3.2 (Note 1)	-	2.4	mA
	0.5	0, 10	10	10	8.0 (Note 1)	-	5.6	mA
	1.5	0, 15	15	26	24 (Note 1)	-	18	mA
Output High Drive Current, I _{OH} Min (Note 2)	4.6	0, 5	5	-0.81	-0.8 (Note 1)	-	-0.48	mA
	2.5	0, 5	5	-2.6	-3.2 (Note 1)	-	-1.55	mA
	9.5	0, 10	10	-2.0	-1.8 (Note 1)	-	-1.18	mA
	13.5	0, 15	15	-5.2	-6.0 (Note 1)	-	-3.1	mA
CD4051B, CD4052B, CD4053B, CD4067B	3, CD4097B	•						
ON-State Resistance, R _{ON} Max (Note 3)	$R_{L} = 10K R$ $V_{DD} - V_{SS}/2$		5	800 (Note 1)	-	1050 (Note 1)	1300 (Note 1)	Ω
	$V_{IS} = V_{SS}$ to	V _{DD}	10	310 (Note 1)	-	400 (Note 1)	500 (Note 1)	Ω
			15	200 (Note 1)	-	240 (Note 1)	320 (Note 1)	Ω
Input Voltage Low, V _{IL} Max (Note 2)	$V_{EE} = V_{SS}$ $R_L = 1K \text{ to } V_{SS}$	V _{SS}	5	1.5 (Note 1)	-	1.5 (Note 1)	1.5 (Note 1)	V
	I _{IS} < 2μΑ		10	3.0		3.0	3.0	V
			15	4.0 (Note 1)	-	4.0 (Note 1)	4.0 (Note 1)	٧
Input Voltage High, V _{IH} Min (Note 2)	$V_{EE} = V_{SS}$ $R_L = 1K \text{ to } V_{SS}$	V _{SS}	5	3.5 (Note 1)	3.5 (Note 1)	-	3.5 (Note 1)	٧
	_{IS} < 2μΑ		10	7.0	7.0	-	7.0	٧
			15	11.0 (Note 1)	11.0 (Note 1)	-	11.0 (Note 1)	٧
Off Channel Leakage Current Any Channel Off Max Note 3)	V _{SS} = 0	V _{EE} = 0	18	±100 (Note 1)	-	±100 (Note 1)	±1000 (Note 1)	nA
Off Channel Leakage Current All Channels (Common Out/In) Off Max (Note 3)	V _{SS} = 0	V _{EE} = 0	18	±100 (Note 1)	-	±100 (Note 1)	±1000 (Note 1)	nA

Non-Standard DC Electrical Specification	s "B" Series Devices (Continued)
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			TE	ST CONDITION	ONS	-55°C	+2	5°C	+125°C	
PARAMETERS			v _o	V _{IN}	V _{DD}	MIN/ MAX	MIN	MAX	MIN/ MAX	UNITS
CD4054B, CD4056B										
Output Low (Sink)	V _{EE}	V _{SS}	-4.5	_	5	0.98	0.8		0.55	mA
Current, I _{OL} (Note 2)	0	0	0.5	-	10	0.98	0.8 (Note 1)	-	0.55	mA
	0	0	1.5	-	15	3.6	2.9 (Note 1)	-	2	mA
Output High (Source) Current, I _{OH} (Note 2)	-5	0	4.5	-	5	-0.6	-0.45 (Note 1)	-	-0.3	mA
	0	0	9.5	-	10	-0.6	-0.45 (Note 1)	-	-0.3	mA
	0 0		13.5	., -	15	-1.9	-1.5 (Note 1)	-	-1.1	mA
CD4066B										
On-State Resistance, R _{ON} Max (Note 3)			$R_{L} = 10K R$ $V_{DD} - V_{SS}/2$ $V_{IS} = V_{SS} to$		5	800 (Note 1)	-	1050 (Note 1)	1300 (Note 1)	Ω
			VIS - VSS to	10				400 (Note 1)	550 (Note 1)	Ω
					15	200 (Note 1)	-	240 (Note 1)	320 (Note 1)	Ω
Control Input Voltage Low, $V_{\rm ILC}$ (Note 2)	, Max		$ \begin{array}{l} V_{ S} = V_{SS,} V_{OS} = V_{DD,} \\ V_{ S} = V_{DD,} V_{OS} = V_{SS} \\ II_{ S}I < 10 \mu A \end{array} $		5	1.0 (Note 1)	-	1.0 (Note 1)	1.0 (Note 1)	٧
					10	2.0	-	2.0	2.0	٧
					15	2.0 (Note 1)	-	2.0 (Note 1)	2.0 (Note 1)	٧
Control Input Voltage High, $V_{\rm IH}$ (Note 2)	_C Min			•	5	3.5 (Note 1)	3.5 (Note 1)	-	3.5 (Note 1)	V
					10	7.0	7.0	-	7.0	V
					15	11.0 (Note 1)	11.0 (Note 1)	-	11.0 (Note 1)	٧
Input/Output Leakage Current Effective Off Resistance $V_C = V_C$			0	0	18	±100	-	±100	±1000	nA
CD4093B										
Positive Trigger Threshold Voltage (Note 3)	V _P Mi	n	,-	(Note 4)	5	2.2 (Note 1)	2.2 (Note 1)	-	2.2 (Note 1)	٧
(14016-0)			-	(Note 4)	10	4.6	4.6	-	4.6	V
			-	(Note 4)	15	6.8 (Note 1)	6.8 (Note 1)	-	6.8 (Note 1)	٧
			-	(Note 5)	5	2.6 (Note 1)	2.6 (Note 1)	-	2.6 (Note 1)	٧
			-	(Note 5)	10	5.6	5.6	-	5.6	V
			-	(Note 5)	15	6.3	6.3	-	6.3	٧

Non-Standard DC Electrical Specifications "B" Series Devices (Continued)

		TE	ST CONDITIO	ONS	-55°C	+25	5°C	+125°C	
PARAMETE	ERS	v _o	V _{IN}	V _{DD}	MIN/ MAX	MIN	МАХ	MIN/ MAX	UNITS
CD4093B (Continued)									
Positive Trigger Threshold Voltage	V _P Max		(Note 4)	5	3.6 (Note 1)	-	3.6 (Note 1)	3.6 (Note 1)	٧
(Note 3)		-	(Note 4)	10	7.1	-	7.1	7.1	٧
			(Note 4)	15	10.8 (Note 1)	-	10.8 (Note 1)	10.8 (Note 1)	V
			(Note 5)	5	4 (Note 1)	-	4 (Note 1)	4 (Note 1)	٧
		-	(Note 5)	10	8.2	-	8.2	8.2	٧
		-	(Note 5)	15	12.7	-	12.7	12.7	٧
Negative Trigger Threshold Voltage (Note 3)	V _N Min	-	(Note 4)	5	0.9 (Note 1)	0.9 (Note 1)	-	0.9 (Note 1)	V
			(Note 4)	10	2.5	2.5	-	2.5	٧
		-	(Note 4)	15	4 (Note 1)	4 (Note 1)	-	4 (Note 1)	٧
		-	(Note 5)	5	1.4 (Note 1)	1.4 (Note 1)	-	1.4 (Note 1)	٧
		-	(Note 5)	10	3.4	3.4	-	3.4	٧
		-	(Note 5)	15	4.8	4.8	-	4.8	٧
	V _N Max	-	(Note 4)	5	2.8 (Note 1)	-	2.8 (Note 1)	2.8 (Note 1)	٧
		-	(Note 4)	10	5.2	-	5.2	5.2	٧
		-	(Note 4)	15	7.4 (Note 1)	-	7.4 (Note 1)	7.4 (Note 1)	٧
			(Note 5)	5	3.2 (Note 1)	-	3.2 (Note 1)	3.2 (Note 1)	٧
		-	(Note 5)	10	6.6	-	6.6	6.6	٧
		-	(Note 5)	15	9.6	-	9.6	9.6	٧
Hysteresis Voltage (Note 3)	V _H Min	-	(Note 4)	5	0.3 (Note 1)	0.3 (Note 1)	-	0.3 (Note 1)	٧
		-	(Note 4)	10	1.2	1.2	-	1.2	V
		-	(Note 4)	15	1.6 (Note 1)	1.6 (Note 1)	-	1.6 (Note 1)	٧
			(Note 5)	5	0.3 (Note 1)	0.3 (Note 1)	-	0.3 (Note 1)	V
		-	(Note 5)	10	1.2	1.2	-	1.2	٧
			(Note 5)	15	1.6	1.6	-	1.6	٧

Non-Standard DC Electrical Specifications "B" Series Devices (Continued)

			TEST CONDITIONS			-55°C	+2	5°C	+125°C	
PARA	METERS		v _o	V _{IN}	V _{DD}	MIN/ MAX	MIN	MAX	MIN/ MAX	UNITS
CD4093B (Continue	ed)									
Hysteresis Voltage (Note 3)				(Note 4)	5	1.6 (Note 1)	-	1.6 (Note 1)	1.6 (Note 1)	٧
			-	(Note 4)	10	3.4	-	3.4	3.4	٧
			-	(Note 4)	15	5 (Note 1)	-	5 (Note 1)	5 (Note 1)	٧
				(Note 5)	5	1.6 (Note 1)	-	1.6 (Note 1)	1.6 (Note 1)	٧
			-	(Note 5)	10	3.4	-	3.4	3.4	٧
				(Note 5)	15	5	-	5	5	٧
CD4502B										
Output Low Drive Cu (Note 2)		0.4	0, 5	5	3.84	3.06 (Note 1)	-	2.16	mA	
			0.5	0, 10	10	9.6	7.8 (Note 1)	-	5.4	mA
	1.5	0, 15	15	25.2	20.4 (Note 1)	-	14.4	mA		
CD4503B										
Output Low Drive Cu (Note 2)	ırrent, I _{OL} Min		0.4	0	5	2.6	2.1 (Note 1)	-	1.3	mA
			0.5	0	10	6.5	5.5 (Note 1)	-	3.8	mA
			1.5	0	15	19.2	16.1 (Note 1)	-	11.2	mA
Output High Drive Co (Note 2)	urrent, I _{OH} Min		4.6	5	5	-1.2	-1.02 (Note 1)	-	-0.7	mA
			2.5	5	5	-5.8	-4.8 (Note 1)	-	-3.0	mA
			9.5	10	10	-3.1	-2.6 (Note 1)	-	-1.8	mA
			13.5	15	15	-8.2	-6.8 (Note 1)	-	-4.8	mA
CD4504B										
		V _{cc}								
Input Low Voltage	TTL-CMOS	5	1	-	10	0.8	-	0.8	0.8	٧
V _{IL} Max (Note 2)	TTL-CMOS	5	1	-	15	0.8 (Note 1)	-	0.8 (Note 1)	0.8 (Note 1)	٧
	CMOS-CMOS	5	1	-	10	1.5 (Note 1)	-	1.5 (Note 1)	1.5 (Note 1)	V
	CMOS-CMOS	5	1.5	-	15	1.5	-	1.5	1.5	٧
	CMOS-CMOS	10	1.5		15	3 (Note 1)	-	3 (Note 1)	3 (Note 1)	V

Non-Standard DC Electrical Specifications "B" Series Devices (Continued)

				TES	TEST CONDITIONS			-55°C +25°C			
PARA	METERS			v _o	V _{IN}	V _{DD}	MIN/ MAX	MIN	MAX	MIN/ MAX	UNITS
CD4504B (Continue	ed)										
Input High Voltage	TTL-CM	os	5	9	-	10	2	2	-	2	V
V _{IH} Min (Note 2)	TTL-CM	os	5	13.5	-	15	2 (Note 1)	2 (Note 1)	-	2 (Note 1)	٧
	CMOS-0	CMOS	5	9		10	3.5 (Note 1)	3.5 (Note 1)	-	3.5 (Note 1)	٧
	CMOS-0	CMOS	5	13.5	-	15	3.5	3.5	-	3.5	٧
	CMOS-0	CMOS	10	13.5		15	7 (Note 1)	7 (Note 1)	-	7 (Note 1)	٧
CD4511B											
Output Voltage High-Level, V _{OH} Min (Note 3)		-	0, 5	5	4	4.1		4.2	٧		
		-	0, 10	10	9	9.1	-	9.2	٧		
		-	0, 15	15	14 (Note 1)	14.1 (Note 1)	-	14.2 (Note 1)	٧		
Output Drive Voltage High 0		_		5	4.0	4.1		4.2	V		
Level, V _{OH} Min (Note 3)			5	-	-	5	-	-	-	-	V
(14010-0)		1	0	-	-	5	3.8	3.9	-	3.9	V
		1	5	-	-	5	-	-	-	3.5	V
		2	0	•	-	5	3.55	3.4 (Note 1)	-	-	٧
		2	5	-	-	5	3.4	3.1	-	-	٧
Output Drive Voltage	High	C)	-	-	10	9.0	9.1	-	9.2	V
Level, V _{OH} Min (Note 3)		5	5	-	-	10		-	-	-	٧
		1	0	-	-	10	8.85	9.0	-	9.0	٧
		1.	5	-	-	10	-	-	-	-	٧
		2	0	-	-	10	8.7	8.6 (Note 1)	-	8.4	٧
		2	5	-	-	10	8.6	8.3	-	-	٧
Output Drive Voltage	High	C)	-	-	15	14.0	14.10		14.20	٧
Level, V _{OH} Min (Note 3)		5	5	-	-	15	-	-		-	V
		1	0	-	-	15	13.90	14.0	-	14.0	V
		1	5	-	-	15	-	-	-	-	٧
		2	0	-	-	15	13.75	13.70 (Note 1)	-	13.50	٧
		2	5	-	-	15	13.65	13.50	-		٧

Non-Standard DC Electrical Specifications "B" Series Devices (Continued)

		TE	ST CONDITION	ONS	-55°C	+2	5°C	+125°C	
PARAMETER	S	v _o	V _{IN}	V _{DD}	MIN/ MAX	MIN	MAX	MIN/ MAX	UNITS
CD4541B									
Output Low Drive Current, I _O (Note 2)	_L Min	0.4	0, 5	5	1.9	1.55 (Note 1)	-	1.08	mA
		0.5	0, 10	10	5.0	4.0 (Note 1)	-	2.8	mA
		1.5	0, 15	15	12.6	10.0 (Note 1)	-	7.2	mA
Output High Drive Current, I_C (Note 2)	_{oH} Min	4.6	0, 5	5	-1.9	-1.55 (Note 1)	-	-1.08	mA
		2.5	0, 5	5	-6.2	-5.0 (Note 1)	-	-3.0	mA
		9.5	0, 10	10	-5.0	-4.0 (Note 1)	-	2.8	mA
		13.5	0, 15	15	-12.6	-10.0 (Note 1)	-	-7.2	mA
CD40106B			America de la constante de la	Annania			-		
Positive Trigger Threshold Voltage (Note 3)	V _P Min	-	-	5	2.2 (Note 1)	2.2 (Note 1)	-	2.2 (Note 1)	٧
		-	-	10	4.6 (Note 1)	4.6 (Note 1)	-	4.6 (Note 1)	٧
			-	15	6.8 (Note 1)	6.8 (Note 1)	-	6.8 (Note 1)	٧
	V _P Max	-	-	5	3.6 (Note 1)	-	3.6 (Note 1)	3.6 (Note 1)	٧
		-	-	10	7.1 (Note 1)	-	7.1 (Note 1)	7.1 (Note 1)	٧
		-	-	15	10.8 (Note 1)	-	10.8 (Note 1)	10.8 (Note 1)	٧
Negative Trigger Threshold Voltage	V _N Min	-	-	5	0.9 (Note 1)	0.9 (Note 1)	-	0.9 (Note 1)	٧
(Note 3)		-	-	10	2.5 (Note 1)	2.5 (Note 1)	-	2.5 (Note 1)	٧
		-	-	15	4 (Note 1)	4 (Note 1)	-	4 (Note 1)	٧
	V _N Max	·	-	5	2.8 (Note 1)	-	2.8 (Note 1)	2.8 (Note 1)	٧
			-	10	5.2 (Note 1)	- 1	5.2 (Note 1)	5.2 (Note 1)	٧
			-	15	7.4 (Note 1)	-	7.4 (Note 1)	7.4 (Note 1)	٧
Hysteresis Voltage (Note 3)	V _H Min		-	5	0.3 (Note 1)	0.3 (Note 1)	-	0.3 (Note 1)	٧
			-	10	1.2 (Note 1)	1.2 (Note 1)	-	1.2 (Note 1)	٧
		-	-	15	1.6 (Note 1)	1.6 (Note 1)	-	1.6 (Note 1)	٧

Non-Standard DC Electrical Specifications "B" Series Devices (Continued)

	TES	T CONDITION	ONS	-55°C	55°C +25°C		+125°C	
PARAMETERS	V _o	V _{IN}	V _{DD}	MIN/ MAX	MIN	MAX	MIN/ MAX	UNITS
CD40106B (Continued)								
Hysteresis Voltage V _H Max (Note 3)	-	-	5	1.6 (Note 1)	-	1.6 (Note 1)	1.6 (Note 1)	٧
	-	-	10	3.4 (Note 1)	-	3.4 (Note 1)	3.4 (Note 1)	٧
	-	-	15	5 (Note 1)	-	5 (Note 1)	5 (Note 1)	٧
CD40107B								
Output Low Current, I _{OL} Min (Note 2)	0.4	0, 5	5	21	16 (Note 1)	-	12	mA
	1	0, 5	5	44	34 (Note 1)	-	25	mA
	0.5	0, 10	10	49	37 (Note 1)	- ,	28	mA
	1	0, 10	10	89	68 (Note 1)	-	51	mA
	0.5	0, 15	15	66	50 (Note 1)	-	38	mA
Output High Current, I _{OH} Min (Note 2)			NO INTE	RNAL PUL	L-UP DEV	CE		
Input Low Voltage, V _{IL} Max	Vo	V _{IN}	V _{DD}					
(Note 2 and Note 6)	4.5	-	5	1.5 (Note 1)	-	1.5 (Note 1)	1.5 (Note 1)	٧
	9		- 10	3.0	-	3.0	3.0	٧
	13.5		15	4.0 (Note 1)	-	4.0 (Note 1)	4.0 (Note 1)	٧
Input High Voltage V _{IH} Max (Notes 2 and 6)	0.5, 4.5	-	5	3.5 (Note 1)	3.5 (Note 1)	-	3.5 (Note 1)	٧
	1, 9	-	10	7.0	7.0	-	7.0	٧
	1.5, 13.5	-	15	11 (Note 1)	11 (Note 1)	-	11 (Note 1)	٧
CD40109B								
Input Low Voltage, V _{IL} Max	Vo	V _{cc}	V _{DD}					
(Note 2)	1, 9	5	10	1.5 (Note 1)	-	1.5 (Note 1)	1.5 (Note 1)	٧
	1.5, 13.5	10	15	3 (Note 1)	-	3 (Note 1)	3 (Note 1)	٧
Input High Voltage, V _{IH} Max (Note 2)	1, 9	5	10	3.5 (Note 1)	3.5 (Note 1)	•	3.5 (Note 1)	٧
	1.5, 13.5	10	15	7 (Note 1)	7 (Note 1)	-	7 (Note 1)	٧

Non-Standard DC Electrical Specifications "B" Series Devices (Continued)

	Material (St. of Carlo States and April (St. of Carlos)	TES	TEST CONDITIONS		-55°C	+2	5°C	+125°C	
PARAMETERS		v _o	V _{IN}	V _{DD}	MIN/ MAX	MIN	мах	MIN/ MAX	UNITS
CD40116									
Quiescent Current (Note 3) From V _{DD} Supply I _{DD} Max		Enable = 1 Enable = 0			6.5 (Note 1)	-	5 (Note 1)	5 (Note 1)	mA
From V _{CC} Supply I _{CC} Max					6.5 (Note 1)	-	5 (Note 1)	5 (Note 1)	mA
					100 (Note 1)	-	100 (Note 1)	200 (Note 1)	μА
DATA FLOW - CMOS INPUTS	TO TTL OUT	PUTS							
Input Current, I _{IN} (Note 2)		V _{IN} = 0, 12\	1		±60 (Note 1)	-	±60 (Note 1)	±60 (Note 1)	μА
Output Current (Note 2)	I _{OH} Min	V _{OH} = 3V, V _{IL} = 2V			-7.5 (Note 1)	-6 (Note 1)	-	-4.2 (Note 1)	mA
TTI Thron State Lookers Curre	I _{OL} Min	V _{OL} = 0.4V, V _{IH} = 10V			7.5 (Note 1)	6 (Note 1)	-	4.2 (Note 1)	mA
TTL Three-State Leakage Current, I _{OUT} Max (Note 2)		Enable = 0			±100 (Note 1)	-	±100 (Note 1)	±100 (Note 1)	μА
DATA FLOW - TTL INPUTS TO	O CMOS OUTF	PUTS							
Input Current (Note 2)	I _{IL} Max	Any TTL Input V _{IL} = 0 to 0.7V V _{IH} = 2.3V			-600 (Note 1)		-500 (Note 1)	-500 (Note 1)	μА
	I _{IH} Max				-450 (Note 1)	•	-350 (Note 1)	-350 (Note 1)	μА
Output Current (Note 2)	I _{OH} Min	V _{OH} = 11.5\	/, V _{IL} = 0.7V		-4.3 (Note 1)	-3.5 (Note 1)	-	-2.5 (Note 1)	mA
	I _{OL} Min	$V_{OL} = 0.5V$,	V _{IH} = 2.3V		4.3 (Note 1)	3.5 (Note 1)	-	2.5 (Note 1)	mA
CMOS Three-State Output Lea (Note 2 and Note 8)	kage Current	V _O = 0, 12V	, V _{IN} = 0, 5V		±60	-	±60	±60	μА
ENABLE AND DISABLE INPU	TS								
Input Current (Note 2)	I _{IL}	V _{IL} = 0 to 0.7V		-600 (Note 1)	-	-500 (Note 1)	-500 (Note 1)	μА	
	I _{IH}	V _{IH} = 2.3V (TTL)		-450 (Note 1)	-	-350 (Note 1)	-350 (Note 1)	μА
	I _{IH}	V _{IH} = 12V (0	CMOS)		60	-	60	60	μА

NOTES:

- 1. These limits are tested 100%.
- 2. Replaces a STD parameter.
- 3. An Additive parameter.
- 4. Input on terminals 1, 5, 8, 12, or 2, 6, 9, 13; other inputs to V_{DD} .
- 5. Input on terminals 1 and 2, 5 and 6, 8 and 9, or 12 and 13; other inputs to V_{DD} .
- 6. Measured with external pull-up resistor, $\rm R_L$ = 10k Ω to $\rm V_{DD}.$
- 7. At -55°C, test is performed with V_{DD} of 18V.
- 8. CMOS Three-State output leakage test is functionally identical to CMOS-to-TTL input current tests.

Switching Characteristics

The table below lists all Harris High-Reliability CD4000B Series devices and shows which switching parameters are 100% tested at final electrical and Group A. In general, Harris tests propagation delay, transition time, and maximum on a one-input to one-output basis only.

clock frequency at 5V where applicable. Harris warrants all other switching parameters shown in the commercial data sheet. Harris High-Reliability switching tests are performed

Switching Characteristics at +25°C

TYPE	(NOTE 1) CONDITIONS V _{DD} = 5V, C _L = 50pF	PROP DELAY (ns)	TRANS TIME (ns)	MAX CLK INPUT FREQ (MHz)
CD4000B	-	250	200	-
CD4000UB	-	120	200	-
CD4001B	-	250	200	-
CD4001UB	-	120	200	-
CD4002B	-	250	200	-
CD4002UB	-	120	200	-
CD4006B	-	400	200	2.5
CD4007UB	-	110	200	-
CD4008B	Sum In to Sum Out	800	200	-
	Carry In to Sum Out	740	-	-
	Sum In to Carry Out	400	-	-
	Carry In to Carry Out	200	-	-
CD4009UB	-	140 (Note 1)	350 (Note 1)	-
	-	60 (Note 2)	70 (Note 2	-
CD4010B	-	200 (Note 1)	350 (Note 1)	
	-	130 (Note 2)	70 (Note 2)	-
CD4011B	-	250	200	-
CD4011UB	-	120	200	-
CD4012B	-	250	200	-
CD4013B	Clock to Q or Q	300	200	3.5
	Set to Q or Reset to Q	300 (Note 1)	-	-
	Set to Q or Reset to Q	400 (Note 2)	-	-
CD4014B	-	320	200	3

TYPE	(NOTE 1) CONDITIONS V _{DD} = 5V, C _L = 50pF	PROP DELAY (ns)	TRANS TIME (ns)	MAX CLK INPUT FREQ (MHz)
CD4015B	Clock to Q	320	200	3
	Reset to Q	400 (Note 2)	-	-
CD4016B	Sig. Input to Sig. Output	100	-	-
11.7	Turn On	70	-	-
CD4017B	Clock to Out	650	200	2.5
	Clock to Carry Out	600	-	-
	Reset to Out	530	-	-
CD4018B	Clock to Q	400	200	3
,	Preset/Reset to Q	550	-	-
CD4019B	-	300	200	-
CD4020B	φ to Q1	360	200	3.5
	Qn to Qn + 1	330	- ,	-
	Reset to Q	280 (Note 2)	-	-
CD4021B	-	320	200	3
CD4022B	Clock to Carry Out	600	200	2.5
	Clock to Decode Out	650	-	
	Reset to Output	530	-	-
CD4023B	-	250	200	-
CD4024B	φ to Q1	360	200	3.5
	Qn to Qn +1	330	-	-
	Reset to Q	280 (Note 2)	-	-
CD4025B	-	250	200	-
CD4025UB	-	120	200	-

TYPE	(NOTE 1) CONDITIONS V _{DD} = 5V, C _L = 50pF	PROP DELAY (ns)	TRANS TIME (ns)	MAX CLK INPUT FREQ (MHz)
CD4027B	Clock to Q or Q	300	200	3.5
	Set to Q or Reset to Q	300 (Note 1)	-	-
	Set to Q or Reset to Q	400 (Note 2)	-	-
CD4028B	-	350	200	-
CD4029B	Q Output	500	200	2
:	Carry Output	560	-	-
	Preset Enable to Q	470	-	-
	Preset Enable to Carry Out	640	-	-
	Carry Input to Carry Out	340	-	-
CD4030B	-	280	200	-
CD4031B	Clock to Q	500	200	2
	Clock to Q	500 (Note 1)	-	-
	Clock to Q	380 (Note 2)	-	-
	Clock to Q'	380	-	-
	Clock to C _{LD}	200	-	-
CD4033B	Clock to Carry Out	500	200	2.5
	Clock to Decode Out	700	-	-
	Reset to Carry Out	550 (Note 1)	-	-
	Reset to Decode Out	600	-	-
CD4034B	Parallel In to Parallel Out	700	200	2
	AE to "A" Out t _{PLZ} , t _{PZL} , t _{PHZ} , t _{PZH}	400	-	-
CD4035B	Clock to Q	500	200	2
	Reset to Q	460	-	-

TYPE	(NOTE 1) CONDITIONS V _{DD} = 5V, C _L = 50pF	PROP DELAY (ns)	TRANS TIME (ns)	MAX CLK INPUT FREQ (MHz)
CD4040B	φ to Q1	360	200	3.5
	Qn to Qn + 1	330	-	-
	Reset to Q	280 (Note 2)	-	-
CD4041UB	-	120	80	-
CD4042B	Data In to Q	220	200	-
	Data In to Q	300	-	-
	Clock to Q	450	-	-
	Clock to Q	500	-	-
CD4043B,	Set or Reset to Q	300	200	-
CD4044B	Enable to Q; t _{PHZ} , t _{PZH}	230	-	
	Enable to Q; t _{PLZ} , t _{PZL}	180	-	-
CD4046B	AC Coupled Signal Input Voltage Sensitivity (Peak to Peak) f _{IN} = 100Hz Sine Wave	360mV Max		
CD4047B	t _R to Q, Q	1000	200	-
	Astable to Q, Q	700	-	-
	Retrigger to Q, Q	600	-	-
	Astable to Oscillator	400	-	-
	Reset to Q, Q	500	-	-
CD4048B	Ka to Output	600	200	-
CD4049UB	-	120 (Note 1)	160 (Note 1)	-
	-	65 (Note 2)	60 (Note 2)	- 1
CD4050B	-	140 (Note 1)	160 (Note 1)	- 7
	-	110 (Note 2)	60 (Note 2)	-
CD4051B	Add to Signal Out	720	-	- 1

TYPE	(NOTE 1) CONDITIONS V _{DD} = 5V, C _L = 50pF	PROP DELAY (ns)	TRANS TIME (ns)	MAX CLK INPUT FREQ (MHz)
CD4052B, CD4053B	Inhibit to Signal Out - Channel On	720	-	-
	Inhibit to Signal Out - Channel Ott	450	-	-
CD4054B	V _{EE} = -5V	800	200	-
CD4056B	V _{EE} = -5V	1300	200	-
CD4060B	Input Pulse Operation ¢I to Q4	740	200	3.5
	Qn to Qn + 1	200	-	-
	Reset Operation	360 (Note 2)	-	-
CD4063B	Comparator Input to Output	1250	200	-
	Cascade Input to Output	1000	-	-
CD4066B	Signal Input to Signal Output $R_L = 200k$, $V_C = V_{DD}$, $V_{SS} = GND$, $V_{IS} = Square Wave \cong 5V and t_R, t_F = 20ns$	40	-	-
	t_{PDC} ; t_{RC} , $t_{FC} = 20$ ns, $R_L = 1$ K and $V_{IS} < 5$ V	70	-	
CD4067B	Add or inhibit to Signal Out Channel On	650	-	-
	Signal In to Out	60	-	-
CD4068B	-	300	200	-
CD4069UB	-	110	200	-
CD4070B	-	280	200	-
CD4071B, CD4072B, CD4073B, CD4075B		250	200	-
CD4076B	Clock to Q	600	200	-
CD4077B	-	280	200	-
CD4078B	-	300	200	3
CD4081B, CD4082B	-	250	200	-

TYPE	(NOTE 1) CONDITIONS V _{DD} = 5V, C _L = 50pF	PROP DELAY (ns)	TRANS TIME (ns)	MAX CLK INPUT FREQ (MHz)
CD4085B, CD4086B	Data	450 (Note 2)	200	-
		620 (Note 1	-	-
	Inhibit	300 (Note 2)	-	-
		500 (Note 1)	-	-
CD4089B	Clock to Out	300	200	1.2
	Clear to Out	760	-	-
	Cascade to Out	180	-	-
CD4093B	-	380	200	-
CD4094B	Clock to Serial Out Qs	600	200	1.25
	Clock to Serial Out Q's	460	-	-
	Clock to Parallel Out	840	-	-
	Strobe to Parallel Out	580	-	-
	Out Enable to Parallel Out, t _{PHZ} , t _{PZH}	280	-	-
	Out Enable to Parallel Out, t _{PLZ} , t _{PZL}	200	-	
CD4095B, CD4096B	Clock to Output	500	200	3.5
CD4096B	Set or Reset	300	-	-
CD4097B	Address or Inhibit to Sig Out - Channel On	650	-	-
	Signal In to Out	60	-	-
CD4098B	Trigger to Q, Q	500	200	-
CD4099B	Data to Output	400	200	-
CD4502B	Data or Inhibit Delay Time	380 (Note 1)	200 (Note 1)	
		270 (Note 2)	120 (Note 2)	-
	Disable Delay Time,	120	-	-
	Disable Delay Time, t _{РZH}	220	-	-

6

CMOS Logic ICs - CD4000B Series

TYPE	(NOTE 1) CONDITIONS V _{DD} = 5V, C _L = 50pF			PROP DELAY (ns)	TRANS TIME (ns)	MAX CLK INPUT FREQ (MHz)
CD4502B (Continued)	Disable Delay t _{PLZ} , t _{PZL}	Time),	250	-	-
CD4503B	-			150 (Note 1)	90 (Note 1)	-
	-		110 (Note 2)	70 (Note 2)	-	
	t _{PHZ} , t _{PZH}			140	-	-
	t _{PLZ} , t _{PZL}			180	-	-
CD4504B	SHIFT MODE	V _{cc}	V _{DD}			
	TTL to CMOS V _{DD} > V _{CC}	5	10	280 (Note 2)	-	-
	CMOS to CMOS V _{DD} > V _{CC}	5	10	240 (Note 2)	-	-
	CMOS to CMOS V _{CC} > V _{DD}	10	5	550 (Note 2)	•	•
	TTL to CMOS V _{DD} > V _{CC}	5	10	280 (Note 1)	-	-
	CMOS to CMOS V _{DD} > V _{CC}	5	10	240 (Note 1)	-	-
	CMOS to CMOS V _{CC} > V _{DD}	10	5	400	-	-
	All Modes	-	5	200	-	-
	[†] ТНС, [†] ТСН	-	10	100	-	-
CD4508B	Strobe In to D	ata O	ut	260	200	-
CD4510B	Clock to Q Ou	tput		400	200	2
	Preset or Reset to Q			420	-	-
	Clock to Carry		480	-	-	
	Carry In to Ca	rry O	ut	250	-	-
	Preset or Res Carry Out	et to		640	-	-

				MAX
TYPE	(NOTE 1) CONDITIONS V _{DD} = 5V, C _L = 50pF	PROP DELAY (ns)	TRANS TIME (ns)	CLK INPUT FREQ (MHz)
CD4511B	Data to Output	1040 (Note 2)	310 (Note 2)	-
	-	1320 (Note 1)	80 (Note 1)	-
CD4512B	Inhibit to Output	280	200	-
	"A" Select to Output	400	-	-
	Data to Output	360	-	-
	t _{PHZ} , t _{PZH}	120	-	-
CD4514B, CD4515B	Strobe or Data	970	200	-
0040100	Inhibit	500	-	-
CD4516B	Clock to Q Output	400	200	2
	Preset or Reset to Q	420	-	-
	Clock to Carry Out	480	-	-
	Carry In to Carry Out	250	-	-
	Preset or Reset to Carry Out	640	-	-
CD4517B	Clock to Q16	400	200	3
CD4518B, CD4520B	Clock to Output	560	200	1.5
0040208	Reset to Output	650 (Note 2)	-	-
CD4527B	Clock to Out	300	200	1.2
	Clear to Out	760	-	-
	Cascade to Out	180	-	-
CD4532B	E _I to E _O , E _I to Gs	220	200	-
	Dn to Qm	440	-	-
	Dn to Gs, E _I to Qm	340	-	-
CD4536B	Clock to Q1 8 Bypass High	2000	200	0.5
	Clock to Q1 8 Bypass Low	5000	-	-
	Clock to Q16	8000	-	-
	Reset to Qn	6000 (Note 2)	-	-

TYPE	(NOTE 1) CONDITIONS V _{DD} = 5V, C _L = 50pF	PROP DELAY (ns)	TRANS TIME (ns)	MAX CLK INPUT FREQ (MHz)
CD4541B	Clock to Q(28)	10500	200 (Note 2)	0.75
	Clock to Q(2 ¹⁶)	18000	360 (Note 1)	-
CD4555B, CD4556B	Select to Any Output	440	200	-
CD4556B	Enable to Any Output	400	-	-
CD4585B	Comparator Inputs to Outputs	600	200	-
	Cascade Inputs to Outputs	400	-	-
CD4724B	Data to Outputs	400	200	-
	Write Disable to Output	400		-
	Reset to Output	350 (Note 2)	-	
	Address to Output	450	-	-
CD14538B	Trigger to Q, Q	600	200	-
	Reset to Q or Q	500	-	-
CD40100B	-	720	200	1
CD40101B	Data In to Output	700	200	-
	Inhibit In to Output	280	-	-
CD40102B, CD40103B	Clock to Output	600	200	0.7
CD40103B	Carry In/Counter Enable to Output	400	-	-
	Asynchronous Preset Enable to Output	1300 (Note 1)		-
	Clear to Output	750 (Note 2)	-	-
CD40104B	Clock to Q	440	200	3
	t _{PZH} , t _{PLZ} , t _{PZL}	160	-	-
	t _{PHZ}	90	-	-
CD40105B	Shift Out or Reset to Data Out Ready	370 (Note 2)	200	1.5
	Shift In to Data In Ready	320 (Note 2)	-	-
	Three-State Control to Data Out t _{PZH}	280	-	-

TYPE	(NOTE 1) CONDITIONS V _{DD} = 5V, C _L = 50pF		PROP DELAY (ns)	TRANS TIME (ns)	MAX CLK INPUT FREQ (MHz)		
CD40105B (Continued)		e Thru D to Out t			4000 (Note 1)	-	-
CD40106B					280	200	-
CD40107B	R _L =	120Ω			200	100	-
CD40108B		or Write)		720	200	1.5
		or Write			600	-	-
	Disat	le Delay t _{PHZ}	Time	,	200	-	-
	Disat	le Delay PLZ	Time	,	260	-	
CD40109B	DATA	INPUT	тоо	UTP	UT		
		HIFT ODE	v _{cc}	V _{DD}			
	L-H L-H		5V	10V	600 (Note 2)	100	-
			5V	10V	260 (Note 1)	-	-
			10V	5V	500 (Note 2)	200	-
		H-L	10V	5V	460 (Note 1)	-	-
	THRE	E-STAT	E DIS	SABL	E DELAY	$R_L = 1k\Omega$!
		SHIFT MODE	v _{cc}	V _{DD}			
	t _{PHZ}	L-H	5V	10V	120	-	-
	t _{PHZ}	H-L	10V	5V	400	-	-
	t _{PLZ}	L-H	5V	10V	740	-	-
	t _{PLZ}	H-L	10V	5V	500	-	-
	t _{PZH}	L-H	5V	10V	640	-	-
	t _{PZH}	H-L	10V	5V	600	-	-
	t _{PZL}	L-H	5V	10V	200	-	-
	t _{PZL}	H-L	10V	5V	400	-	-

Switching Characteristics at +25°C (Continued)

TYPE	(NOTE 1) CONDITIONS V _{DD} = 5V, C _L = 50pF	PROP DELAY (ns)	TRANS TIME (ns)	MAX CLK INPUT FREQ (MHz)
CD40116	Data In to Data Out, CMOS In, TTL Out	35	40	-
	Data in to Data Out, TTL In, CMOS Out	45	-	-
	Disable to TTL Out, t _{PHZ} , t _{PLZ}	45	-	-
	Disable to TTL Out, t _{PZH} , t _{PZL}	50	-	-
	Enable to CMOS Out, t _{PHZ} , t _{PLZ}	30	-	-
	Enable to CMOS Out, t _{PZH} , t _{PZL}	60	-	-
CD40160B, CD40161B,	Clock to Q	400	200	2
CD40161B, CD40163B	Clock to C _{OUT}	450	-	-
	T _E to C _{OUT}	250	-	-
	Clear to Q (CD40160B and CD40161B Only)	500 (Note 2)	-	-
CD40174B	Clock to Output	300	200	3.5
	Clear to Output	200 (Note 2)		-

TYPE	(NOTE 1) CONDITIONS V _{DD} = 5V, C _L = 50pF	PROP DELAY (ns)	TRANS TIME (ns)	MAX CLK INPUT FREQ (MHz)
CD40192B, CD40193B	Clock Up or Clock Down to Q, Reset Q	500	200	2
	PE to Q	400	-	-
	Clock Up to Carry, Clock Down to Borrow	320	-	-
	Reset or PE to Borrow or Carry	600	-	-
CD40194B	Clock to Q	440	200	3
	Reset to Q	460 (Note 2)	-	-
CD40257B	Data Input to Output	300	200	-
	Select to Output	380		-
	Output Disable to Output	-	-	-
	t _{PZH} , t _{PHZ}	190	-	-
	t _{PZL} , t _{PLZ}	190	-	-

NOTES:

- 1. t_{TLH} or t_{PLH}
- 2. t_{THL} or t_{PHL}

Gate Count

TYPE NUMBER	GATE COUNT
CD4000B	12
CD4000UB	4
CD4001B	10
CD4001UB	4
CD4002B	9
CD4002UB	4
CD4006B	83
CD4007UB	2
CD4008B	34
CD4009UB	8
CD4010B	8
CD4011B	10
CD4011UB	4
CD4012B	9
CD4013B	20
CD4014B	57
CD4015B	54
CD4016B	6
CD4017B	50
CD4018B	40
CD4019B	10
CD4020B	85
CD4021B	57
CD4022B	40
CD4023B	11
CD4023UB	5
CD4024B	45
CD4025B	11
CD4025UB	5
CD4027B	25
CD4028B	26
CD4029B	64
CD4030B	11
CD4031B	271
CD4033B	72
CD4034B	106
CD4035B	45
CD4040B	75
CD4041UB	8
CD4042B	16
	23

TYPE NUMBER	GATE COUNT
CD4044B	23
CD4046B	35
CD4047B	46
CD4048B	28
CD4049UB	3
CD4050B	6
CD4051B	58
CD4052B	40
CD4053B	46
CD4054B	28
CD4056B	70
CD4060B	83
CD4063B	56
CD4066B	9
CD4067B	75
CD4068B	11
CD4069UB	3
CD4070B	11
CD4071B	12
CD4072B	11
CD4073B	12
CD4075B	12
CD4076B	54
CD4077B	11
CD4078B	11
CD4081B	12
CD4082B	11
CD4085B	10
CD4086B	9
CD4089B	67
CD4093B	14
CD4094B	88
CD4095B	19
CD4096B	19
CD4097B	74
CD4098B	37
CD4099B	62
CD4502B	26
CD4503B	17
CD4504B	20
CD4508B	48

TYPE NUMBER	GATE COUNT
CD4510B	65
CD4511B	55
CD4512B	20
CD4514B	59
CD4515B	67
CD4516B	58
CD4517B	280
CD4518B	72
CD4520B	71
CD4527B	63
CD4532B	28
CD4536B	195
CD4541B	119
CD4555B	21
CD4556B	25
CD4585B	40
CD4724B	62
CD14538B	58
CD40100B	173
CD40101B	27
CD40102B	141
CD40103B	139
CD40104B	52
CD40105B	242
CD40106B	18
CD40107B	4
CD40108B	137
CD40109B	72
CD40116	76
CD40160B	66
CD40161B	66
CD40163B	66
CD40174B	37
CD40175B	28
CD40192B	80
CD40193B	87
CD40194B	52
CD40257B	35

NOTE

 Gate Count is based on four transistors per gate rounded off to nearest nondecimal integer.

Static Life Test and Burn-In Test Circuit Connections (Note 1 and Note 2)

	STATIC BURN-IN			
TYPE	OPEN	GND	V _{DD}	
CD4000	1, 2, 6, 9, 10	7	3-5, 8, 11-14	
CD4001	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12-14	
CD4002	1, 6, 8, 13	7	2-5, 9-12, 14	
CD4006	2, 8-13	7	1, 3-6, 14	
CD4007	1, 5, 8, 12, 13	4, 7, 9	2, 3, 6, 10, 11, 14	
CD4008	10-14	8	1-7, 9, 15, 16	
CD4009 (Note 3)	2, 4, 6, 10, 12, 13, 15	8	1 (Note 4), 3, 5, 7, 9, 11, 14, 16 (Note 4)	
CD4010 (Note 3)	2, 4, 6, 10, 12, 13, 15	8	1 (Note 4), 3, 5, 7, 9, 11, 14, 16 (Note 4)	
CD4011	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12-14	
CD4012	1, 6, 8, 13	7	2-5, 9-12, 14	
CD4013	1, 2, 12, 13	7	3-6, 8-11, 14	
CD4014	2, 3, 12	8	1, 4-7, 9-11, 13-16	
CD4015	2-5, 10-13	8	1, 6, 7, 9, 14-16	
CD4016	2, 3, 9, 10	7	1, 4-6, 8, 11-14	
CD4017	1-7, 9-12	8, 14	13, 15, 16	
CD4018	4-6, 11, 13	8	1-3, 7, 9, 10, 12, 14-16	
CD4019	10-13	8	1-7, 9, 14-16	
CD4020	1-7, 9, 12-15	8	10, 11, 16	
CD4021	2, 3, 12	8	1, 4-7, 9-11, 13-16	
CD4022	1-7, 9-12	8, 14	13, 15, 16	
CD4023	6, 9, 10	7	1-5, 8, 11-14	
CD4024	3-6, 8-13	7	1, 2, 14	
CD4025	6, 9, 10	7	1-5, 8, 11-14	
CD4027	1, 2, 14, 15	8	3-7, 9-13, 16	
CD4028	1-7, 9, 14, 15	8	10-13, 16	
CD4029	2, 6, 7, 11, 14	8	1, 3-5, 9, 10, 12, 13, 15, 16	
CD4030	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12-14	
CD4031	3-7, 9, 11-14	8	1, 2, 10, 15, 16	
CD4033	4-7, 9-13	8	1-3, 14-16	
CD4034	1-8	12	9-11, 13-24	
CD4035	1, 13-15	8	2-7, 9-12, 16	
CD4040	1-7, 9, 12-15	8	10, 11, 16	

	STATIC BURN-IN				
TYPE	OPEN	GND	V _{DD}		
CD4041	1, 2, 4, 5, 8, 9, 11, 12	7	3, 6, 10, 13, 14		
CD4042	1-3, 9-12, 15	8	4-7, 13, 14, 16		
CD4043	1, 2, 9, 10, 13	8	3-7, 11, 12, 14-16		
CD4044	1, 2, 9, 10, 13	8	3-7, 11, 12, 14-16		
CD4046	1, 2, 4, 6, 7, 10, 11, 13, 15	8	3, 5, 9, 12, 14, 16		
CD4047	1, 2, 10, 11, 13	7	3-6, 8, 9, 12, 14		
CD4048	1	8	2-7, 9-16		
CD4049 (Note 3)	2-4, 6, 10, 12, 13, 15	8	1 (Note 4), 3, 5, 7, 9, 11, 14, 16 (Note 4)		
CD4050 (Note 3)	2, 4, 6, 10, 12, 13, 15	8	1 (Note 4), 3, 5, 7, 9, 11, 14, 16 (Note 4)		
CD4051 (Note 3)	3	7 (Note 4), 8 (Note 4)	1, 2, 4-6, 9-16		
CD4052 (Note 3)	3, 13	7 (Note 4), 8 (Note 4)	1, 2, 4-6, 9-12, 14-16		
CD4053 (Note 3)	4, 14, 15	7 (Note 4), 8 (Note 4)	1-3, 5, 6, 9-13, 16		
CD4054 (Note 3)	3-6	7 (Note 4), 8	1, 2, 9-16		
CD4056 (Note 3)	9-15	7 (Note 4), 8	1-6, 16		
CD4060	1-7, 9, 10, 13-15	8	11, 12, 16		
CD4063	5-7	3, 8	1, 2, 4, 9-16		
CD4066	2, 3, 9, 10	7	1, 4-6, 8, 11-14		
CD4067	1	12	2-11, 13-23		
CD4068	1, 6, 8, 13	7	2-5, 9-12, 14		
CD4069	2, 4, 6, 8, 10, 12	7	1, 3, 5, 9, 11, 13, 14		
CD4070	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12-14		
CD4071	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12-14		
CD4072	1, 6, 8, 13	7	2-5, 9-12, 14		
CD4073	6, 9, 10	7	1-5, 8, 11-14		
CD4075	6, 9, 10	7	1-5, 8, 11-14		
CD4076	3-6	8	1, 2, 7, 9-16		
CD4077	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12-14		
CD4078	1, 6, 8, 13	7	2-5, 9-12, 14		

Static Life Test and Burn-In Test Circuit Connections (Continued)

		STATIC BURN-IN			
	TYPE	OPEN	GND	V _{DD}	
С	D4081	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12-14	
С	D4082	1, 6, 8, 13	7	2-5, 9-12, 14	
С	D4085	3, 4	7	1, 2, 5, 6, 8-14	
C	D4086	3, 4	7	1, 2, 5, 6, 8-14	
С	D4089	1, 5-7	8	2-4, 9-16	
С	D4093	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12-14	
С	D4094	4-7, 9-14	8	1-3, 15, 16	
С	D4095	1, 6, 8	7	2-5, 9-14	
С	D4096	1, 6, 8	7	2-5, 9-14	
С	D4097	1, 17	12	2-11, 13-24	
С	D4098	2, 6, 7, 9, 10, 14	1, 8, 15	3-5, 11-13, 16	
С	D4099	1, 9-15	8	2-7, 16	
С	D4502	2, 5, 7, 9, 11, 14	8	1, 3, 4, 6, 10, 12, 13, 15, 16	
С	D4503	3, 5, 7, 9, 11, 13	8	1, 2, 4, 6, 10, 12, 14-16	
С	D4504	2, 4, 6, 10, 12, 15	8	16, (1 [Note 4], 3, 5, 7, 9, 11, 13, 14), Note 5	
С	D4508	5, 7, 9, 11, 17, 19, 21, 23	12	1-4, 6, 8, 10, 13-16, 18, 20, 22, 24	
С	D4510	2, 6, 7, 11, 14	8	1, 3-5, 9, 10, 12, 13, 15, 16	
С	D4511	9-15	8	1-7, 16	
С	D4512	14	8	1-7, 9-13, 15, 16	
С	D4514	4-11, 13-20	12	1-3, 21-24	
С	D4515	4-11, 13-20	12	1-3, 21-24	
С	D4516	2, 6, 7, 11, 14	8	1, 3-5, 9, 10, 12, 13, 15, 16	
С	D4517	1, 2, 5, 6, 10, 11, 14, 15	8	3, 4, 7, 9, 12, 13, 16	
С	D4518	3-6, 11-14	8	1, 2, 7, 9, 10, 15, 16	
С	D4520	3-6, 11-14	8	1, 2, 7, 9, 10, 15, 16	
С	D4527	1, 5-7	8	2-4, 9-16	
С	D4532	6, 7, 9, 14, 15	8	1-5, 10-13, 16	
C	D4536	4, 5, 13	8	1-3, 6, 7, 9-12, 14-16	
CI	D4541	1, 2, 4, 8, 11	7	3, 5, 6, 9, 10, 12-14	
CI	D4555	4-7, 9-12	8	1-3, 13-16	
CI	D4556	4-7, 9-12	8	1-3, 13-16	

	STATIC BURN-IN				
TYPE	OPEN	GND	V _{DD}		
CD4585	3, 12, 13	8	1, 2, 4-7, 9-11, 14-16		
CD4724	4-7, 9-12	8	1, 3, 13-16		
CD14538	2, 6, 7, 9, 10, 14	1, 8, 15	3-5, 11-13, 16		
CD40100	1, 4, 5, 7, 10, 12, 14, 15	8	2, 3, 6, 9, 11, 13, 16		
CD40101	6, 9	7	1-5, 8, 10-14		
CD40102	14	8	1-7, 9-13, 15, 16		
CD40103	14	8	1-7, 9-13, 15, 16		
CD40104	12-15	8	1-7, 9-11, 16		
CD40105	2, 10-14	8	1, 3-7, 9, 15, 16		
CD40106	2, 4, 6, 8, 10, 12	7	1, 3, 5, 9, 11, 13, 14		
CD40107	1, 2, 5, 6, 8, 9, 12, 13	7	3, 4, 10, 11, 14		
CD40108	1, 2, 4-7, 22, 23	12	3, 8-11, 13-21, 24		
CD40109 (Note 3)	4, 5, 11-13	8	16, (1 [Note 4], 2, 3, 6, 7, 9, 10, 14, 15), Note 5		
CD40116 (Note 3)	2-9	11, 12	1 (Note 4) 10 = V _{DD} (Note 6) 13-22 (Note 4) = V _{CC}		
CD40160	11-15	8	1-7, 9, 10, 16		
CD40161	11-15	8	1-7, 9, 10, 16		
CD40163	11-15	8	1-7, 9, 10, 16		
CD40174	2, 5, 7, 10, 12, 15	8	1, 3, 4, 6, 9, 11, 13, 14, 16		
CD40175	2, 3, 6, 7, 10, 11, 14, 15	8	1, 4, 5, 9, 12, 13, 16		
CD40193	2, 3, 6, 7, 12, 13	8	1, 4, 5, 9-11, 14-16		
CD40194	12-15	8	1-7, 9-11, 16		
CD40257	4, 7, 9, 12	8, 15	1-3, 5, 6, 10, 11, 13, 14, 16		

NOTES:

- 1. For Type A devices, use V_{DD} = 12.5V. For Type B and UB devices, use V_{DD} = 18V.
- 2. Each pin except V_{DD} and V_{SS} must have resistors of $2k\Omega$ to $47k\Omega$. In most cases, V_{SS} is at pin 7 (of a 14 pin IC), pin 8 (of a 16 pin IC) or pin 12 (of a 24 pin IC), while V_{DD} is at the highest numbered pin; exceptions are noted.
- 3. Non-standard pin arrangement, or multiple supply pins.
- 4. Connect pin(s) without using resistor.
- 5. Pin voltage is $V_{DD}/2$ for pins inside parentheses.
- 6. V_{DD} = 11.5V; V_{CC} = 6.5V; use 300Ω resistors at pins 10, 13-21.

additional device in the (sub)lot represented by the sample shall be tested on the same test setup for all parameters in that test, subgroup, or set of tests/subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/ subgroups. as applicable. For class S only, if this testing results in a percent defective greater than 5%, the (sub)lot shall be rejected, except that for (sub)lot previously unscreened to the tests that caused failure of this percent defective, the (sub)lot may be accepted by resubmission and passing the failed individual tests, subgroups, or set of test/subgroups, as applicable, using a 116/0 sample. Electrical Test Requirements for Non-JAN

5. If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every

Quality Assurance and Reliability

MIL-STD-883, Notice 5

GROUP A ELECTRICAL TESTS FOR CLASS B (JAN) DEVICES (NOTE 1)

SUBGROUPS (NOTE 2) QUALITY/ACCEPT NO. = 116/0 (NOTES 3, 4 AND 5)

Subgroup 1

DC Test at +25°C

Subgroup 2

DC Tests at Maximum Rated Operating Temperature

DC Tests at Minimum Rated Operating Temperature

Subgroup 4

AC Tests at +25°C

Subgroup 5

AC Tests at Maximum Rated Operating Temperature

AC Tests at Minimum Rated Operating Temperature

Functional Tests at +25°C

Functional Tests at Maximum Rated Operating Temperature

Functional Tests at Minimum Rated Operating Temperature

Switching Tests at +25°C

Switching Tests at Maximum Rated Operating Temperature

Switching Tests at Minimum Rated Operating Temperature

NOTES: (Group A)

- 1. The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.
- 2. At the manufacturer's option, the applicable test required for group A testing (see Note 1) may be conducted individually or combined into sets of tests, subgroups (as defined in the Group A Electrical Tests Table), or sets of subgroups. However, the manufacturer shall predesignate these groupings prior to grouping a testing. Unless otherwise specified, the individual tests. subgroups, or sets of test/subgroups may be performed in any sequence.
- 3. The sample plan (quantity and accept number) for each test, subgroup, or set of tests/subgroups as predesignated in Note 2 above, shall be 116/0.
- 4. A greater sample size may be used at the manufacturer's option; however, the accept number shall remain at zero. When the (sub)lot size is less than the required sample size, each and every device in the (sub)lot shall be inspected and all failed devices removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable.

Lot Conformance Tests

GROUP A ELECTRICAL TESTS FOR HARRIS 3, 3A AND SMD PRODUCT

	SUB GROUPS W	HERE USED
	Subgroup 1All Types W DC Tests at +25°C	hen Required
	Subgroup 2	hen Required
	Subgroup 3All Types W DC Tests at Minimum Rated Operating Temperature	hen Required
	Subgroup 7All Types W Functional Tests at +25°C	hen Required
	Subgroup 8A	hen Required
	Subgroup 8B	hen Required
	Subgroup 9Digital Types W	hen Required

CD4000 3, 3A AND SMD

Switching Tests at +25°C

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (PER METHOD 5005, GROUP A ELECTRICAL TESTS TABLE)
Group A Test Requirements (Method 5005)	1, 2, 3, 7, 8, 9
Groups B and C End-Point Electrical Parameter (Method 5005) (Class S and B)	1, 2, 3, 7, 8
Groups D End-Point Electrical Parameters (Method 5005)	1, 2, 3

Life Test Reliability Data

Reliability can be defined as "the probability of a device performing a function, under specific conditions for which designed, for a specific period of time." But because of the higher reliability levels required in today's integrated circuits, the extended time and high cost required to measure their reliability at application stress levels become prohibitive.

A practical method of meeting these concerns is through the use of accelerated life testing, a method by which devices are operated at, or subjected to, higher stress levels than they normally experience in a typical application.

Life tests are generally performed at elevated temperatures and maximum recommended operating voltage in order to accelerate time-dependent failure mechanisms related to conditions of temperature and electrical stress. Life testing is the principal method used in predicting the failure rates of components in actual field applications.

Activation Energy

The activation energy is defined as the minimum kinetic energy a molecule or atom in the initial state of a process must acquire before it can take part in a reaction. Failure mechanisms can differ markedly in terms of their reaction rates. A low activation energy implies that the reaction rate (failure rate) will not be accelerated as much by temperature as will a reaction with a high activation energy.

The acceleration factor used in predicting the failure rate from the life test condition depends directly on the activation energy.

The activation energy estimates reported in the semiconductor industry, as obtained from integrated circuit life test evaluations, fall in the range of approximately 0.3eV to 1.4eV. However, a value of 1.0eV has been shown to be fairly representative. This value has been demonstrated on Harris Logic CMOS integrated circuits using relatively large sample quantities and is the value used in Calculating Life Test Temperature Acceleration Factors.

Temperature Acceleration Factor

A variety of failure mechanisms can be accelerated by life testing. The reaction rates of most of these mechanisms are highly dependent of temperature and are best expressed by the Arrhenius model:

$$R(T) = A \exp(-E/kT)$$

where,

R(T) = Reaction Rate

A = Constant

k = Boltzmann's Constant (8.63 x 10-5eV/oK)

E = Activation Energy (eV)

T = Absolute Temperature (°C +273)

For electronic components, the reaction rate refers to the failure rate. The acceleration factor, which relates the test failure rate to the end-use failure rate, can be determined from the Arrhenius equation for any activation energy, as follows:

$$F_{A} = exp\left[\frac{E}{k}\left(\frac{1}{T_{USE}} - \frac{1}{T_{TEST}}\right)\right]$$

Reliability Data

						FOUR	FAILURE AT 60% U	
PRODUCT CLASSIFICATION	QUANTITY TESTED	ACTUAL DEVICE HRS	TEST TEMP.	TEST VOLTS	NO. REJECTS	DEVICE HRS AT +55°C	%/1000 HRS AT +55°C	FITS AT +55°C
CD4000B-JAN B	4326	2,180,304	135	18	12	2.2 X 10 ⁹	6.1 X 10 ⁻⁴	6.1
CD4000A-JAN B	4209	2,121,336	135	12.5	14	2.2 X 10 ⁹	7.2 X 10 ⁻⁴	7.2
CD4000B 3A	539	539,000	125	18	0	1.1 X 10 ⁹	3.6 X 10 ⁻⁴	3.6
	722	861,000	135	18	3	1.1 X 10 ⁹	3.6 X 10 ⁻⁴	3.6
CD4000B 3	4280	4,280,000	125	18	0	5.7 X 10 ⁹	1.1 X 10 ⁻⁴	1.1
	7060	3,530,000	135	18	5	5.7 X 10 ⁹	1.1 X 10 ⁻⁴	1.1
CD4000A 3	2387	2,387,000	125	12.5	0	4.2 X 10 ⁹	0.73 X 10 ⁻⁴	0.7
	5920	2,960,000	135	12.5	2	4.2 X 10 ⁹	0.73 X 10 ⁻⁴	0.7

CMOS LOGIC ICs

PRODUCT SELECTION GUIDE

PACKAGING INFORMATION

	PAGE
LOGIC PACKAGE SELECTION GUIDE.	7-3
CERAMIC DUAL-IN-LINE METAL SEAL PACKAGES (SBDIP)	7-17
DUAL-IN-LINE PLASTIC PACKAGES (PDIP)	7-19
CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGES (CERDIP)	7-24
CERAMIC METAL SEAL FLATPACK PACKAGES (FLATPACK)	7-26
SMALL OUTLINE PLASTIC PACKAGES (SOIC)	7-28
SHRINK SMALL OUTLINE PLASTIC PACKAGES (SSOP)	7-30

- Logic Package Selection Guide -

Using the Selection Guide

The first character of each entry indicates the package type, while the number preceding the decimal point details the package lead count. The entire entry indicates the package table containing the appropriate package dimensions (e.g. 14 lead PDIP dimensions are detailed in Table E14.3). The index on page 7-1 lists page numbers for CerDIP, Flatpack, PDIP, Sidebraze, SOIC and SSOP tables.

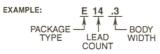
PART NUMBERS	CERDIP	FLATPACK	PDIP	SIDEBRAZE	SOIC	SSOP
CD54HC/HCT00	F14.3					
CD54HC/HCT02	F14.3					
CD54HC/HCT03	F14.3					
CD54HC/HCT04	F14.3					
CD54HC/HCT08	F14.3					
CD54HC/HCT10	F14.3					
CD54HC/HCT11	F14.3					
CD54HC/HCT14	F14.3					
CD54HC/HCT20	F14.3					
CD54HC/HCT27	F14.3					
CD54HC/HCT30	F14.3					
CD54HC/HCT32	F14.3					
CD54HC/HCT73	F14.3					
CD54HC/HCT74	F14.3					
CD54HC/HCT85	F16.3					
CD54HC/HCT86	F14.3					
CD54HC/HCT107	F14.3					
CD54HC/HCT112	F16.3					
CD54HC/HCT123	F16.3		,			
CD54HC/HCT125	F14.3					
CD54HC/HCT126	F14.3					
CD54HC/HCT132	F14.3					
CD54HC/HCT138	F16.3					
CD54HC/HCT139	F16.3					
CD54HC/HCT147	F16.3					
CD54HC/HCT151	F16.3					
CD54HC/HCT153	F16.3					
CD54HC/HCT154	F24.6					
CD54HC/HCT157	F16.3					
CD54HC/HCT161	F16.3					
CD54HC/HCT163	F16.3					
CD54HC/HCT164	F14.3					
CD54HC/HCT165	F16.3					

PART NUMBERS	CERDIP	FLATPACK	PDIP	SIDEBRAZE	SOIC	SSOP
CD54HC/HCT166	F16.3					activated be little to be because the many
CD54HC/HCT173	F16.3					
CD54HC/HCT174	F16.3					
CD54HC/HCT175	F16.3					
CD54HC/HCT190	F16.3					
CD54HC/HCT191	F16.3					
CD54HC/HCT193	F16.3					
CD54HC194	F16.3					
CD54HC/HCT221	F16.3					
CD54HC/HCT237	F16.3					
CD54HC/HCT238	F16.3					
CD54HC/HCT240	F20.3					
CD54HCT241	F20.3					
CD54HC/HCT243	F14.3					
CD54HC/HCT244	F20.3					
CD54HC/HCT245	F20.3					
CD54HC/HCT251	F16.3					
CD54HC/HCT257	F16.3					
CD54HC/HCT259	F16.3					
CD54HC/HCT273	F20.3					
CD54HC/HCT280	F14.3					
CD54HC/HCT283	F16.3					
CD54HC/HCT299	F20.3					
CD54HC/HCT366	F16.3					
CD54HC/HCT367	F16.3					
CD54HC/HCT368	F16.3					
CD54HC/HCT373	F20.3					
CD54HC/HCT374	F20.3					
CD54HC/HCT377	F20.3					
CD54HCT390	F16.3					
CD54HC/HCT393	F14.3					
CD54HC/HCT423	F16.3					
CD54HC/HCT540	F20.3					
CD54HC/HCT541	F20.3					
CD54HC/HCT564	F20.3					
CD54HC/HCT573	F20.3					
CD54HC/HCT574	F20.3					
CD54HC/HCT597	F16.3					



PART NUMBERS	CERDIP	FLATPACK	PDIP	SIDEBRAZE	SOIC	SSOP
CD54HC/HCT646	F24.6					
CD54HC/HCT670	F16.3					
CD54HC/HCT688	F20.3					
CD54HC/HCT4015	F16.3					
CD54HC/HCT4017	F16.3					
CD54HC/HCT4020	F16.3					
CD54HC/HCT4024	F16.3					
CD54HC/HCT4040	F16.3					
CD54HC/HCT4046A	F16.3					
CD54HC/HCT4051	F16.3					
CD54HC/HCT4052	F16.3					
CD54HC/HCT4053	F16.3					
CD54HC/HCT4060	F16.3					
CD54HC/HCT4066	F14.3					
CD54HCT4067	F24.6					
CD54HC/HCT4094	F16.3					
CD54HC/HCT4511	F16.3					
CD54HC/HCT4514	F24.6					
CD54HC/HCT4518	F16.3					
CD54HC/HCT4520	F16.3					
CD54HC/HCT4538	F16.3					
CD54HC7266	F14.3					
CD54HC/HCT40102	F16.3					
CD54HC/HCT40103	F16.3					
CD54HC/HCT40105	F16.3					
CD74HC/HCT00			E14.3		M14.15	
CD74HC/HCT02			E14.3		M14.15	
CD74HC/HCT03			E14.3		M14.15	
CD74HC/HCT04			E14.3		M14.15	
CD74HC/HCT08			E14.3		M14.15	
CD74HC/HCT10			E14.3		M14.15	
CD74HC/HCT11			E14.3		M14.15	
CD74HC/HCT14	~		E14.3		M14.15	
CD74HC/HCT20			E14.3		M14.15	
CD74HC/HCT21			E14.3		M14.15	
CD74HC/HCT27			E14.3		M14.15	
CD74HC/HCT30			E14.3		M14.15	
CD74HC/HCT32			E14.3		M14.15	

PART NUMBERS	CERDIP	FLATPACK	PDIP	SIDEBRAZE	SOIC	SSOP
CD74HC/HCT42			E16.3		M16.15	
CD74HC/HCT73			E14.3		M14.15	
CD74HC/HCT74			E14.3		M14.15	
CD74HC/HCT75			E16.3		M16.15	
CD74HC/HCT85			E16.3		M16.15	
CD74HC/HCT86			E14.3		M14.15	
CD74HC/HCT93			E14.3		M14.15	
CD74HC/HCT107			E14.3		M14.15	
CD74HC/HCT109			E16.3		M16.15	
CD74HC/HCT112			E16.3		M16.15	
CD74HC/HCT123			E16.3		M16.15	
CD74HC/HCT125			E14.3		M14.15	
CD74HC/HCT126			E14.3		M14.15	
CD74HC/HCT132			E14.3		M14.15	
CD74HC/HCT137			E16.3		M16.15	
CD74HC/HCT138			E16.3		M16.15	
CD74HC/HCT139			E16.3		M16.15	
CD74HC/HCT147			E16.3		M16.15	
CD74HC/HCT151			E16.3		M16.15	
CD74HC/HCT153			E16.3		M16.15	
CD74HC/HCT154			E24.3 E24.6		M24.3	
CD74HC/HCT157			E16.3		M16.15	
CD74HC/HCT158			E16.3		M16.15	
CD74HC/HCT160			E16.3		M16.15	
CD74HC/HCT161			E16.3		M16.15	
CD74HC/HCT162			E16.3		M16.15	
CD74HC/HCT163			E16.3		M16.15	
CD74HC/HCT164			E14.3		M14.15	
CD74HC/HCT165			E16.3		M16.15	
CD74HC/HCT166			E16.3	-	M16.15	
CD74HC/HCT173			E16.3		M16.15	
CD74HC/HCT174			E16.3		M16.15	
CD74HC/HCT175			E16.3		M16.15	
CD74HC/HCT181			E24.3 E24.6			
CD74HC/HCT190			E16.3		M16.15	
CD74HC/HCT191			E16.3		M16.15	
CD74HC/HCT192			E16.3		M16.15	



PART NUMBERS	CERDIP	FLATPACK	PDIP	SIDEBRAZE	SOIC	SSOP
CD74HC/HCT193			E16.3		M16.15	
CD74HC/HCT194			E16.3		M16.15	
CD74HC/HCT195			E16.3		M16.15	
CD74HC/HCT221			E16.3		M16.15	
CD74HC/HCT237			E16.3		M16.15	
CD74HC/HCT238			E16.3		M16.15	
CD74HC/HCT240			E20.3		M20.3	
CD74HC/HCT241			E20.3		M20.3	
CD74HC/HCT242			E14.3		M14.15	
CD74HC/HCT243			E14.3		M14.15	
CD74HC/HCT244			E20.3		M20.3	
CD74HC/HCT245			E20.3		M20.3	
CD74HC/HCT251			E16.3		M16.15	
CD74HC/HCT253			E16.3		M16.15	
CD74HC/HCT257			E16.3		M16.15	
CD74HC/HCT258			E16.3		M16.15	
CD74HC/HCT259			E16.3		M16.15	
CD74HC/HCT273			E20.3		M20.3	
CD74HC/HCT280			E14.3		M14.15	
CD74HC/HCT283			E16.3		M16.15	
CD74HC/HCT297			E16.3			
CD74HC/HCT299			E20.3		M20.3	
CD74HC/HCT354			E20.3			
CD74HC/HCT356			E20.3			
CD74HC/HCT365			E16.3		M16.15	
CD74HC/HCT366			E16.3		M16.15	
CD74HC/HCT367			E16.3		M16.15	
CD74HC/HCT368			E16.3		M16.15	
CD74HC/HCT373			E20.3		M20.3	
CD74HC/HCT374			E20.3		M20.3	
CD74HC/HCT377			E20.3		M20.3	
CD74HC/HCT390			E16.3		M16.15	
CD74HC/HCT393			E14.3		M14.15	
CD74HC/HCT423			E16.3		M16.15	
CD74HC/HCT533			E20.3			
CD74HC/HCT534			E20.3		M20.3	
CD74HC/HCT540			E20.3		M20.3	
CD74HC/HCT541			E20.3		M20.3	



PART NUMBERS	CERDIP	FLATPACK	PDIP	SIDEBRAZE	SOIC	SSOP
CD74HC/HCT563			E20.3		M20.3	
CD74HC/HCT564			E20.3		M20.3	
CD74HC/HCT573			E20.3		M20.3	
CD74HC/HCT574			E20.3		M20.3	
CD74HC/HCT583			E16.3			
CD74HC/HCT597			E16.3		M16.15	
CD74HC/HCT640			E20.3		M20.3	
CD74HC/HCT643			E20.3			
CD74HC/HCT646			E24.3 E24.6		M24.3	
CD74HC/HCT648			E24.3		M24.3	
CD74HC/HCT670			E16.3		M16.15	
CD74HC/HCT688			E20.3		M20.3	
CD74HC/HCT4002			E14.3		M14.15	
CD74HC/HCT4015			E16.3		M16.15	
CD74HC/HCT4016			E14.3			
CD74HC/HCT4017			E16.3		M16.15	
CD74HC/HCT4020			E16.3		M16.15	
CD74HC/HCT4024			E14.3		M14.15	
CD74HC/HCT4040			E16.3		M16.15	
CD74HC/HCT4046A			E16.3		M16.15	
CD74HC4049			E16.3		M16.15	
CD74HC4050			E16.3		M16.15	
CD74HC/HCT4051			E16.3		M16.15	
CD74HC/HCT4052			E16.3		M16.15	
CD74HC/HCT4053			E16.3		M16.15	
CD74HC/HCT4059			E24.3 E24.6		M24.3	
CD74HC/HCT4060			E16.3		M16.15	
CD74HC/HCT4066			E14.3		M14.15	
CD74HC/HCT4067			E24.3		M24.3	
CD74HC/HCT4075			E14.3		M14.15	
CD74HC/HCT4094			E16.3		M16.15	
CD74HC/HCT4316			E16.3		M16.15	
CD74HC/HCT4351			E20.3		M20.3	
CD74HC/HCT4352	1		E20.3		M20.3	
CD74HC/HCT4353			E20.3			
CD74HC/HCT4510					M16.15	
CD74HC/HCT4511	1	1	E16.3	1	M16.15	



PART NUMBERS	CERDIP	FLATPACK	PDIP	SIDEBRAZE	SOIC	SSOP
CD74HC/HCT4514			E24.3 E24.6		M24.3	
CD74HC/HCT4515			E24.3 E24.6		M24.3	
CD74HC/HCT4516			E16.3		M16.15	
CD74HC/HCT4518			E16.3		M16.15	
CD74HC/HCT4520			E16.3		M16.15	
CD74HC/HCT4538			E16.3		M16.15	
CD74HC/HCT4543			E16.3			
CD74HC/HCT7030			E28.6			
CD74HC/HCT7046A			E16.3		M16.15	
CD74HC7266			E14.3		M14.15	
CD74HC/HCT40102			E16.3		M16.15	
CD74HC/HCT40103			E16.3		M16.15	
CD74HC/HCT40104					M16.15	
CD74HC/HCT40105			E16.3		M16.15	
CD74HCU04			E14.3		M14.15	
CD54AC/ACT00F3A	F14.3					
CD54AC/ACT02F3A	F14.3					
CD54AC/ACT04F3A	F14.3					
CD54AC/ACT05F3A	F14.3					
CD54AC/ACT08F3A	F14.3					
CD54ACT20F3A	F14.3					
CD54AC/ACT32F3A	F14.3					
CD54AC/ACT74F3A	F14.3					
CD54ACT86F3A	F14.3					
CD54AC/ACT109F3A	F16.3					
CD54AC/ACT112F3A	F16.3					
CD54AC/ACT138F3A	F16.3					
CD54AC/ACT139F3A	F16.3					
CD54ACT151F3A	F16.3					
CD54AC/ACT153F3A	F16.3					
CD54AC157F3A	F16.3					
CD54AC/ACT161F3A	F16.3					
CD54AC/ACT163F3A	F16.3					
CD54AC/ACT164F3A	F14.3					
CD54ACT174F3A	F16.3					
CD54AC/ACT191F3A	F16.3					
CD54AC/ACT193F3A	F16.3	1			, , , , , , , , , , , , , , , , , , , ,	

PART NUMBERS	CERDIP	FLATPACK	PDIP	SIDEBRAZE	SOIC	SSOP
CD54AC/ACT240F3A	F20.3					
CD54ACT241F3A	F20.3					
CD54AC/ACT244F3A	F20.3					
CD54AC/ACT245F3A	F20.3					
CD54ACT253F3A	F16.3					
CD54AC/ACT257F3A	F16.3					
CD54AC/ACT273F3A	F20.3					
CD54AC/ACT280F3A	F14.3					
CD54AC/ACT283F3A	F16.3					
CD54AC/ACT299F3A	F20.3					
CD54ACT323F3A	F20.3					
CD54AC/ACT373F3A	F20.3					
CD54AC/ACT374F3A	F20.3					
CD54ACT533F3A	F20.3					
CD54AC/ACT534F3A	F20.3					
CD54ACT540F3A	F20.3					
CD54AC/ACT541F3A	F20.3					
CD54AC/ACT573F3A	F20.3					
CD54AC/ACT574F3A	F20.3					
CD54ACT623F3A	F20.3					
CD74AC/ACT00			E14.3		M14.15	
CD74AC/ACT02			E14.3		M14.15	
CD74AC/ACT04			E14.3		M14.15	
CD74AC/ACT05			E14.3		M14.15	
CD74AC/ACT08			E14.3		M14.15	
CD74AC/ACT10			E14.3		M14.15	
CD74AC/ACT14			E14.3		M14.15	
CD74AC/ACT20			E14.3		M14.15	
CD74AC/ACT32			E14.3		M14.15	
CD74AC/ACT74			E14.3		M14.15	
CD74AC/ACT86			E14.3		M14.15	
CD74AC/ACT109			E16.3		M16.15	
CD74AC/ACT112			E16.3		M16.15	
CD74AC/ACT138			E16.3		M16.15	
CD74AC/ACT139			E16.3		M16.15	
CD74AC/ACT151			E16.3		M16.15	
CD74AC/ACT153			E16.3		M16.15	
CD74AC/ACT157			E16.3		M16.15	



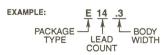
PART NUMBERS	CERDIP	FLATPACK	PDIP	SIDEBRAZE	SOIC	SSOP
CD74AC/ACT158			E16.3		M16.15	
CD74AC/ACT161			E16.3		M16.15	
CD74AC/ACT163			E16.3		M16.15	
CD74AC/ACT164			E14.3		M14.15	
CD74AC/ACT174			E16.3		M16.15	
CD74AC/ACT175			E16.3		M16.15	
CD74AC/ACT191			E16.3		M16.15	
CD74AC/ACT193			E16.3		M16.15	
CD74AC/ACT238			E16.3		M16.15	
CD74AC/ACT240			E20.3		M20.3	
CD74AC/ACT241			E20.3		M20.3	
CD74AC/ACT244			E20.3		M20.3	M20.209
CD74AC/ACT245			E20.3		M20.3	M20.209
CD74AC/ACT251			E16.3			
CD74AC/ACT253			E16.3		M16.15	
CD74AC/ACT257			E16.3		M16.15	M16.209
CD74AC/ACT258			E16.3		M16.15	
CD74AC/ACT273			E20.3		M20.3	M20.209
CD74AC/ACT280			E14.3		M14.15	
CD74AC/ACT283			E16.3		M16.15	
CD74AC/ACT297					M16.15	
CD74AC/ACT299			E20.3		M20.3	
CD74AC/ACT323			E20.3			
CD74AC/ACT373			E20.3		M20.3	
CD74AC/ACT374			E20.3		M20.3	
CD74AC/ACT533			E20.3		M20.3	
CD74AC/ACT534			E20.3		M20.3	
CD74AC/ACT540			E20.3		M20.3	
CD74AC/ACT541			E20.3		M20.3	M20.209
CD74AC/ACT563			E20.3		M20.3	
CD74AC/ACT564			E20.3		M20.3	
CD74AC/ACT573			E20.3		M20.3	
CD74AC/ACT574			E20.3		M20.3	
CD74AC/ACT623			E20.3		M20.3	
CD74AC/ACT646			E24.3		M24.3	M24.209
CD74AC/ACT647					M24.3	
CD74AC/ACT648			E24.3		M24.3	
CD74AC/ACT651		1	E24.3		M24.3	1

PART NUMBERS	CERDIP	FLATPACK	PDIP	SIDEBRAZE	SOIC	SSOP
CD74AC/ACT652			E24.3		M24.3	
CD74AC/ACT653					M24.3	
CD74AC/ACT654			E24.3		angene un quantitate garanten di regionne i la familia di la diligió filo con quantan per	
CD74AC/ACT7060			E20.3		M20.3	
CD74AC/ACT7623			E20.3		M20.3	
CD74FCT240			E20.3		M20.3	M20.209
CD74FCT241			E20.3		M20.3	
CD74FCT244			E20.3		M20.3	M20.209
CD74FCT245			E20.3		M20.3	M20.209
CD74FCT273			E20.3		M20.3	
CD74FCT373			E20.3		M20.3	
CD74FCT374			E20.3		M20.3	M20.209
CD74FCT533					M20.3	
CD74FCT540			E20.3		M20.3	
CD74FCT541			E20.3		M20.3	M20.209
CD74FCT543			E24.3		M24.3	M24.209
CD74FCT564			E20.3		M20.3	
CD74FCT573			E20.3		M20.3	M20.209
CD74FCT574			E20.3		M20.3	M20.209
CD74FCT623					M20.3	
CD74FCT646			E24.3		M24.3	M24.209
CD74FCT651			E24.3		M24.3	
CD74FCT652			E24.3		M24.3	
CD74FCT653			E24.3		M24.3	
CD74FCT654			E24.3		M24.3	
CD74FCT821A			E24.3		M24.3	
CD74FCT822A			E24.3			
CD74FCT823A			E24.3			
CD74FCT824A			E24.3			
CD74FCT841A			E24.3		M24.3	
CD74FCT842A					M24.3	
CD74FCT843A			E24.3		M24.3	
CD74FCT844A			E24.3			
CD74FCT861A					M24.3	
CD74FCT863A					M24.3	
CD74FCT2952A					M24.3	
CD74FCT7623					M20.3	
CD4001B	F14.3	K14.B	E14.3	D14.3		

PART NUMBERS	CERDIP	FLATPACK	PDIP	SIDEBRAZE	SOIC	SSOP
CD4001UB	F14.3		E14.3	D14.3		
CD4002B	F14.3	K14.B	E14.3	D14.3		
CD4006B	F14.3		E14.3	D14.3		
CD4007UB	F14.3		E14.3	D14.3		
CD4008B	F16.3	K16.D	E16.3	D16.3		
CD4009UB	F16.3	K16.D	E16.3	D16.3		
CD4010B	F16.3	K16.D	E16.3	D16.3		
CD4011B	F14.3	K14.B	E14.3	D14.3	are regered to the transport and the territories	
CD4011UB	F14.3		E14.3	D14.3		
CD4012B	F14.3	K14.B	E14.3	D14.3		
CD4013B	F14.3	K14.B	E14.3	D14.3		
CD4014B	F16.3	K16.D	E16.3	D16.3		
CD4015B	F16.3	K16.D	E16.3	D16.3		
CD4016B	F14.3	K14.B	E14.3	D14.3		
CD4017B	F16.3	K16.D	E16.3	D16.3		
CD4018B	F16.3	K16.D	E16.3	D16.3		
CD4019B	F16.3	K16.D	E16.3	D16.3	Aldersamon entrepo e Aliques a entrepo e Aliques a entrepo e Aliques	
CD4020B	F16.3	K16.D	E16.3	D16.3		
CD4021B	F16.3	K16.D	E16.3	D16.3		
CD4022B	F16.3		E16.3	D16.3		
CD4023B	F14.3	K14.B	E14.3	D14.3	TENNOTO CONTROL CONTRO	
CD4024B	F14.3	K14.B	E14.3	D14.3		
CD4025B	F14.3		E14.3	D14.3	Strokkowerphorphicoan belikeredo-do-vondenantw	
CD4026B	F16.3		E16.3			
CD4027B	F16.3	K16.D	E16.3	D16.3		
CD4028B	F16.3	K16.D	E16.3	D16.3		
CD4029B	F16.3	K16.D	E16.3	D16.3		
CD4030B	F14.3	K14.B	E14.3	D14.3		
CD4031B	F16.3	K16.D	E16.3	D16.3		
CD4033B			E16.3	D16.3		
CD4034B	F24.6		E24.6	D24.6		
CD4035B	F16.3	K16.D	E16.3	D16.3		
CD4040B	F16.3	K16.D	E16.3	D16.3		
CD4041UB	F14.3	K14.B	E14.3	D14.3		
CD4042B	F16.3	K16.D	E16.3	D16.3		
CD4043B	F16.3		E16.3	D16.3		
CD4044B	F16.3		E16.3	D16.3		
CD4045B			E16.3			



PART NUMBERS	CERDIP	FLATPACK	PDIP	SIDEBRAZE	SOIC	SSOP
CD4046B	F16.3	K16.D	E16.3	D16.3		
CD4047B	F14.3		E14.3	D14.3		
CD4048B	F16.3		E16.3	D16.3		
CD4049UB	F16.3	K16.D	E16.3	D16.3		
CD4050B	F16.3	K16.D	E16.3	D16.3		
CD4051B	F16.3	K16.D	E16.3	D16.3		
CD4052B	F16.3	K16.D	E16.3	D16.3		
CD4053B	F16.3		E16.3	D16.3		
CD4054B	F16.3		E16.3			
CD4055B			E16.3			
CD4056B	F16.3		E16.3			
CD4059A	F24.6		E24.6	D24.6		
CD4060B	F16.3		E16.3	D16.3		
CD4063B	F16.3	K16.D	E16.3	D16.3		
CD4066B	F14.3	K14.B	E14.3	D14.3		
CD4067B	F24.6		E24.6	D24.6		
CD4068B	F14.3		E14.3	D14.3		
CD4069UB	F14.3	K14.B	E14.3	D14.3		
CD4070B	F14.3		E14.3	D14.3		
CD4071B	F14.3	K14.B	E14.3	D14.3		
CD4072B	F14.3		E14.3	D14.3		
CD4073B	F14.3		E14.3	D14.3		
CD4075B	F14.3	K14.B	E14.3	D14.3		
CD4076B	F16.3		E16.3	D16.3		
CD4077B	F14.3		E14.3	D14.3		
CD4078B	F14.3		E14.3	D14.3		
CD4081B	F14.3	K14.B	E14.3	D14.3		
CD4082B	F14.3		E14.3	D14.3		
CD4085B	F14.3		E14.3	D14.3		
CD4086B	F14.3		E14.3	D14.3		
CD4089B	F16.3		E16.3	D16.3		
CD4093B	F14.3	K14.B	E14.3	D14.3		
CD4094B	F16.3		E16.3	D16.3		
CD4095B	F14.3		E14.3	D14.3		
CD4096B	F14.3		E14.3	D14.3		
CD4097B	F24.6		E24.6	D24.6		
CD4098B	F16.3	K16.D	E16.3	D16.3		
CD4099B	F16.3	K16.D	E16.3	D16.3		



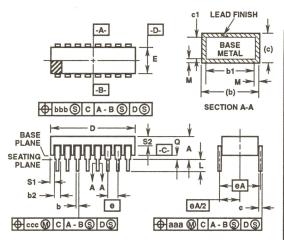
PART NUMBERS	CERDIP	FLATPACK	PDIP	SIDEBRAZE	SOIC	SSOP
CD4502B	F16.3	K16.D	E16.3	D16.3		
CD4503B	F16.3	K16.D	E16.3	D16.3		
CD4504B	F16.3		E16.3	D16.3		
CD4508B	F24.6	K24.D	E24.6	D24.6		
CD4510B	F16.3		E16.3	D16.3		
CD4511B	F16.3	K16.D	E16.3	D16.3		
CD4512B	F16.3		E16.3	D16.3		
CD4514B	F24.6		E24.6	D24.6		
CD4515B	F24.6		E24.6	D24.6		
CD4516B	F16.3	K16.D	E16.3	D16.3		
CD4517B	F16.3		E16.3	D16.3		
CD4518B	F16.3		E16.3	D16.3		
CD4519B	F16.3		E16.3			
CD4520B	F16.3	K16.D	E16.3	D16.3		
CD4521B	F16.3		E16.3			
CD4522B	F16.3		E16.3			
CD4527B	F16.3		E16.3	D16.3		
CD4529B	F16.3		E16.3		THE STATE OF THE S	
CD4532B	F16.3		E16.3	D16.3		
CD4536B	F16.3		E16.3	D16.3		
CD4541B	F14.3		E14.3			
CD4543B			E16.3			
CD4555B	F16.3	K16.D	E16.3	D16.3	Areana saaraa ahaa ahaa ahaa ahaa ahaa ahaa a	
CD4556B	F16.3		E16.3	D16.3		
CD4560B	F16.3		E16.3			
CD4566B			E16.3			
CD4572UB			E16.3			
CD4585B	F16.3		E16.3	D16.3		
CD4724B	E16.3		E16.3			
CD7211			E40.6			
CD7211A			E40.6			
CD7211AM			E40.6			
CD7211M			E40.6			
CD14538B	F16.3		E16.3	D16.3		
CD22402			E24.6	D24.6		
CD22777			E8.3			
CD40100B			E16.3	D16.3		
CD40102B	F16.3		E16.3	D16.3		

PACKAGE PACKAGE LEAD WIDTH

PART NUMBERS	CERDIP	FLATPACK	PDIP	SIDEBRAZE	SOIC	SSOP
CD40103B	F16.3		E16.3	D16.3		
CD40105B	F16.3	K16.D	E16.3	D16.3		
CD40106B		K14.B	E14.3	D14.3		
CD40107B	F14.3		E8.3	D14.3		
CD40109B	F16.3	K16.D	E16.3	D16.3		
CD40110B			E16.3			
CD40116			E22.4	D22.4		
CD40117B			E14.3			
CD40147B	F16.3		E16.3			
CD40160B	F16.3		E16.3			
CD40161B	F16.3		E16.3	D16.3		
CD40163B	F16.3		E16.3	D16.3		
CD40174B	F16.3		E16.3	D16.3		
CD40175B	F16.3		E16.3			
CD40192B	F16.3		E16.3	D16.3		
CD40193B	F16.3		E16.3	D16.3		
CD40194B		K16.D	E16.3	D16.3		
CD40257B	F16.3		E16.3	D16.3		



Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

- Index area: A notch or a pin one identification mark shall be located ed adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
- The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
- Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
- Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
- Dimension Q shall be measured from the seating plane to the base plane.
- 6. Measure dimension S1 at all four corners.
- Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
- 8. N is the maximum number of terminal positions.
- 9. Braze fillets shall be concave.
- 10. Dimensioning and tolerancing per ANSI Y14.5M 1982.
- 11. Controlling dimension: INCH.

D16.3 MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C) 16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL MIN MAX MIN MAX NOT A - 0.200 - 5.08 - b 0.014 0.026 0.36 0.66 2 b1 0.014 0.023 0.36 0.58 3 b2 0.045 0.065 1.14 1.65 - b3 0.023 0.045 0.58 1.14 4 c 0.008 0.018 0.20 0.46 2 c1 0.008 0.015 0.20 0.38 3 D - 0.840 - 21.34 - E 0.220 0.310 5.59 7.87 - e 0.100 BSC 2.54 BSC - eA 0.300 BSC 7.62 BSC - eA/2 0.150 BSC 3.81 BSC - L 0.125 0.200 3.18 5.08 - Q 0.015 0.060 0.38	ES
b 0.014 0.026 0.36 0.66 2 b1 0.014 0.023 0.36 0.58 3 b2 0.045 0.065 1.14 1.65 - b3 0.023 0.045 0.58 1.14 4 c 0.008 0.018 0.20 0.46 2 c1 0.008 0.015 0.20 0.38 3 D - 0.840 - 21.34 - E 0.220 0.310 5.59 7.87 - e 0.100 BSC 2.54 BSC - eA 0.300 BSC 7.62 BSC - eA/2 0.150 BSC 3.81 BSC - L 0.125 0.200 3.18 5.08 -	
b1 0.014 0.023 0.36 0.58 3 b2 0.045 0.065 1.14 1.65 - b3 0.023 0.045 0.58 1.14 4 c 0.008 0.018 0.20 0.46 2 c1 0.008 0.015 0.20 0.38 3 D - 0.840 - 21.34 - E 0.220 0.310 5.59 7.87 - e 0.100 BSC 2.54 BSC - eA 0.300 BSC 7.62 BSC - eA/2 0.150 BSC 3.81 BSC - L 0.125 0.200 3.18 5.08 -	
b2 0.045 0.065 1.14 1.65 - b3 0.023 0.045 0.58 1.14 4 c 0.008 0.018 0.20 0.46 2 c1 0.008 0.015 0.20 0.38 3 D - 0.840 - 21.34 - E 0.220 0.310 5.59 7.87 - e 0.100 BSC 2.54 BSC - eA 0.300 BSC 7.62 BSC - eA/2 0.150 BSC 3.81 BSC - L 0.125 0.200 3.18 5.08 -	
b3 0.023 0.045 0.58 1.14 4 c 0.008 0.018 0.20 0.46 2 c1 0.008 0.015 0.20 0.38 3 D - 0.840 - 21.34 - E 0.220 0.310 5.59 7.87 - e 0.100 BSC 2.54 BSC - eA 0.300 BSC 7.62 BSC - eA/2 0.150 BSC 3.81 BSC - L 0.125 0.200 3.18 5.08 -	
c 0.008 0.018 0.20 0.46 2 c1 0.008 0.015 0.20 0.38 3 D - 0.840 - 21.34 - E 0.220 0.310 5.59 7.87 - e 0.100 BSC 2.54 BSC - eA 0.300 BSC 7.62 BSC - eA/2 0.150 BSC 3.81 BSC - L 0.125 0.200 3.18 5.08 -	
c1 0.008 0.015 0.20 0.38 3 D - 0.840 - 21.34 - E 0.220 0.310 5.59 7.87 - e 0.100 BSC 2.54 BSC - eA 0.300 BSC 7.62 BSC - eA/2 0.150 BSC 3.81 BSC - L 0.125 0.200 3.18 5.08 -	
D - 0.840 - 21.34 - E 0.220 0.310 5.59 7.87 - e 0.100 BSC 2.54 BSC - eA 0.300 BSC 7.62 BSC - eA/2 0.150 BSC 3.81 BSC - L 0.125 0.200 3.18 5.08 -	
E 0.220 0.310 5.59 7.87 - e 0.100 BSC 2.54 BSC - eA 0.300 BSC 7.62 BSC - eA/2 0.150 BSC 3.81 BSC - L 0.125 0.200 3.18 5.08 -	
e 0.100 BSC 2.54 BSC - eA 0.300 BSC 7.62 BSC - eA/2 0.150 BSC 3.81 BSC - L 0.125 0.200 3.18 5.08 -	
eA 0.300 BSC 7.62 BSC - eA/2 0.150 BSC 3.81 BSC - L 0.125 0.200 3.18 5.08 -	
eA/2 0.150 BSC 3.81 BSC - L 0.125 0.200 3.18 5.08 -	
L 0.125 0.200 3.18 5.08 -	
Q 0.015 0.060 0.38 1.52 5	
S1 0.005 - 0.13 - 6	
S2 0.005 - 0.13 - 7	
α 90° 105° 90° 105° -	
aaa - 0.015 - 0.38 -	
bbb - 0.030 - 0.76 -	
ccc - 0.010 - 0.25 -	
M - 0.0015 - 0.038 2	
N 16 16 8	

Rev. 0 4/94

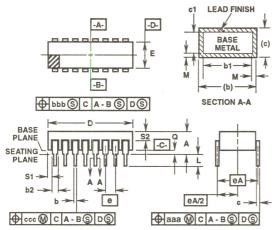
D14.3 MIL-STD-1835 CDIP2-T14 (D-1, CONFIGURATION C) 14 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

	INC	HES	MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	-	0.200		5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
С	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D		0.785	-	19.94	-
E	0.220	0.310	5.59	7.87	-
е	0.100	0.100 BSC		BSC	-
eA	0.300	BSC	7.62 BSC		-
eA/2	0.150	BSC	3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010		0.25	-
М	-	0.0015	-	0.038	2
N	1	4	1	4	8

Rev. 0 4/94

Packaging Outlines

Ceramic Dual-In-Line Metal Seal Packages (SBDIP) (Continued)



NOTES:

- Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
- The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
- Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
- Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
- Dimension Q shall be measured from the seating plane to the base plane.
- 6. Measure dimension S1 at all four corners.
- Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
- 8. N is the maximum number of terminal positions.
- 9. Braze fillets shall be concave.
- 10. Dimensioning and tolerancing per ANSI Y14.5M 1982.
- 11. Controlling dimension: INCH.

D24.6 MIL-STD-1835 CDIP2-T24 (D-3, CONFIGURATION C) 24 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

	INC	HES	MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
С	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.290	-	32.77	-
E	0.500	0.610	12.70	15.49	-
е	0.100	0.100 BSC		2.54 BSC	
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300	0.300 BSC		7.62 BSC	
L	0.120	0.200	3.05	5.08	
Q	0.015	0.075	0.38	1.91	5
S1	0.005	· -	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
М	-	0.0015	-	0.038	2
N	2	4	2	4	8

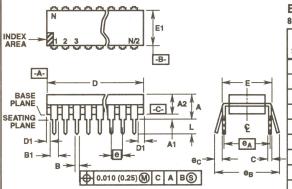
Rev. 0 4/94

D22.4 MIL-STD-1835 CDIP2-T22 (D-7, CONFIGURATION C) 22 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

	INC	HES	MILLIM	ETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES	
Α		0.225	-	5.72	-	
b	0.014	0.026	0.36	0.66	2	
b1	0.014	0.023	0.36	0.58	3	
b2	0.045	0.065	1.14	1.65	-	
b3	0.023	0.045	0.58	1.14	4	
С	0.008	0.018	0.20	0.46	2	
c1	0.008	0.015	0.20	0.38	3	
D	-	1.111	-	28.22	-	
E	0.350	0.410	8.89	10.41	-	
е	0.100	0.100 BSC		2.54 BSC		
eA	0.400 BSC		10.16 BSC		-	
eA/2	0.200	0.200 BSC		5.08 BSC		
L	0.125	0.200	3.18	5.08	-	
Q	0.015	0.070	0.38	1.78	5	
S1	0.005	-	0.13	-	6	
S2	0.005	-	0.13	-	7	
α	90°	105°	90°	105°	-	
aaa	-	0.015	-	0.38	-	
bbb	-	0.030	-	0.76	-	
ccc	-	0.010	-	0.25	-	
М	-	0.0015	-	0.038	2	
N	2	2	2	2	8	

Rev. 0 4/94

Dual-In-Line Plastic Packages (PDIP)



NOTES:

- 1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- 2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
- 3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- 4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- 5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- 6. E and eA are measured with the leads constrained to be perpendicular to datum -C-
- 7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
- 8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- 9. N is the maximum number of terminal positions.
- 10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D) **8 LEAD DUAL-IN-LINE PLASTIC PACKAGE**

	INC	HES	MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
В	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	- 1	0.13	-	5
E	0.300	0.325	7.62	8.25	6 .
E1	0.240	0.280	6.10	7.11	5
е	0.100	BSC	2.54	BSC	-
Θ _A	0.300	BSC	7.62	BSC	6
e _B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8	3	1	3	9
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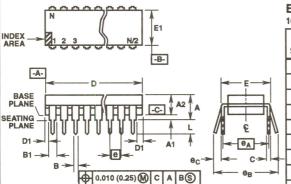
E14.3 (JEDEC MS-001-AA ISSUE D) 14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

	INC	HES	MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
В	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
С	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
е	0.100	BSC	2.54	BSC	-
e _A	0.300	BSC	7.62 BSC		6
e _B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	1	4	1	4	9

Rev. 0 12/93

Packaging Outlines

Dual-In-Line Plastic Packages (PDIP) (Continued)



NOTES:

- Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- 2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
- 3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- 4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
- 7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
- B1 maximum dimensions do not include dambar protrusions.
 Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- 9. N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

	INCHES MILLIMETERS				
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
В	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
С	0.008	0.014	0.204	0.355	-
. D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
е	0.100	BSC	2.54	BSC	-
θ _A	0.300	BSC	7.62 BSC		6
ΘB	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	1	6	1	6	9

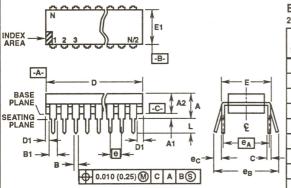
Rev. 0 12/93

E20.3 (JEDEC MS-001-AD ISSUE D) 20 LEAD DUAL-IN-LINE PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
В	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.55	1.77	8
С	0.008	0.014	0.204	0.355	-
D	0.980	1.060	24.89	26.9	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
ө	0.100 BSC		2.54 BSC		-
θ _A	0.300 BSC		7.62 BSC		6
e _B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	20		20		9

Rev. 0 12/93

Dual-In-Line Plastic Packages (PDIP) (Continued)



NOTES:

- Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- 2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
- 3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
- e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
- B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- 9. N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E22.4 (JEDEC MS-010-AA ISSUE C)
22 LEAD DUAL-IN-LINE PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
В	0.014	0.022	0.356	0.558	-
B1	0.045	0.065	1.15	1.65	8
C	0.009	0.015	0.229	0.381	-
. D	1.065	1.120	27.06	28.44	5
D1	0.005	-	0.13	-	5
Е	0.390	0.425	9.91	10.79	6
E1	0.330	0.390	8.39	9.90	5
е	0.100 BSC		2.54 BSC		-
e _A	0.400 BSC		10.16 BSC		6
e _B		0.500	-	12.70	7
L	0.115	0.160	2.93	4.06	4
N	22		22		9

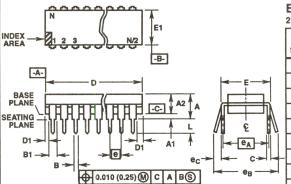
Rev. 0 12/93

E24.3 (JEDEC MS-001-AF ISSUE D)
24 LEAD NARROW BODY DUAL-IN-LINE PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
А	-	0.210	-	5.33	4
A1	0.015		0.39	-	4
A2	0.115	0.195	2.93	4.95	-
В	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
С	0.008	0.014	0.204	0.355	-
D	1.230	1.280	31.24	32.51	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
е	0.100 BSC		2.54 BSC		-
e _A	0.300 BSC		7.62 BSC		6
e _B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	24		24		9

Rev. 0 12/93

Dual-In-Line Plastic Packages (PDIP) (Continued)



NOTES:

- Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- 2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
- 7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
- B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- 9. N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 0.045 inch (0.76 1.14mm).

E24.6 (JEDEC MS-011-AA ISSUE B)
24 LEAD DUAL-IN-LINE PLASTIC PACKAGE

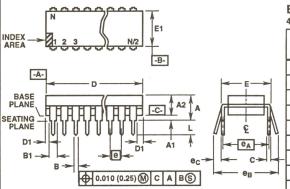
	INC	HES	MILLIM	ETERS	
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
В	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
С	0.008	0.015	0.204	0.381	-
D	1.150	1.290	29.3	32.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
е	0.100	BSC	2.54	BSC	-
e _A	0.600	BSC	15.24	BSC	6
e _B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	2	4	2	4	9

Rev. 0 12/93

E28.6 (JEDEC MS-011-AB ISSUE B) 28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

	INCHES MILLIMETERS		MILLIM	ETERS	
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
В	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
С	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
е	0.100	BSC	2.54	BSC	-
e _A	0.600	BSC	15.24	BSC	6
e _B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	2	8	. 2	8	9

Dual-In-Line Plastic Packages (PDIP) (Continued)



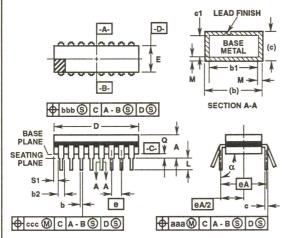
NOTES:

- Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- 2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- 7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
- B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- 9. N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E40.6 (JEDEC MS-011-AC ISSUE B)
40 LEAD DUAL-IN-LINE PLASTIC PACKAGE

	INC	HES	MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
В	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
С	0.008	0.015	0.204	0.381	
D	1.980	2.095	50.3	53.2	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
е	0.100	BSC	2.54	BSC	-
e _A	0.600	BSC	15.24	BSC	6
e _B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	4	0	4	.0	9

Ceramic Dual-In-Line Frit Seal Packages (CerDIP)



NOTES:

- Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
- The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
- Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
- Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
- This dimension allows for off-center lid, meniscus, and glass overrun.
- Dimension Q shall be measured from the seating plane to the base plane.
- 7. Measure dimension S1 at all four corners.
- 8. N is the maximum number of terminal positions.
- 9. Dimensioning and tolerancing per ANSI Y14.5M 1982.
- 10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

	INC	HES	MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	
b3	0.023	0.045	0.58	1.14	4
С	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
е	0.100	BSC	2.54 BSC		-
eA	0.300	BSC	7.62 BSC		-
eA/2	0.150	BSC	3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030		0.76	-
ccc	-	0.010	-	0.25	
М		0.0015	-	0.038	2,3
N	1	6	1	6	8

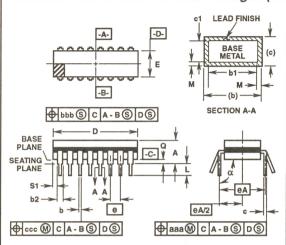
Rev. 0 4/94

F14.3 MIL-STD-1835 GDIP1-T14 (D-1, CONFIGURATION A)
14 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE)

14 LEAD CEHAMIC DUAL-IN-LINE PHIT SEAL PACKAGE)						
	INC	HES	MILLIM	ETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES	
Α	-	0.200		5.08		
b	0.014	0.026	0.36	0.66	2	
b1	0.014	0.023	0.36	0.58	3	
b2	0.045	0.065	1.14	1.65	-	
b3	0.023	0.045	0.58	1.14	4	
С	0.008	0.018	0.20	0.46	2	
c1	0.008	0.015	0.20	0.38	3	
D	-	0.785	-	19.94	5	
E	0.220	0.310	5.59	7.87	5	
е	0.100	BSC	2.54 BSC		-	
eA	0.300	BSC	7.62 BSC		-	
eA/2	0.150	BSC	3.81	BSC	-	
L	0.125	0.200	3.18	5.08	-	
Q	0.015	0.060	0.38	1.52	6	
S1	0.005	-	0.13	-	7	
α	90°	105°	90°	105°	-	
aaa	-	0.015	-	0.38	-	
bbb	•	0.030	-	0.76	-	
ccc	-	0.010	-	0.25		
М	-	0.0015	-	0.038	2,3	
N	1	4	1	4	8	

Rev. 0 4/94

Ceramic Dual-In-Line Frit Seal Packages (CerDIP) (Continued)



NOTES:

- Index area: A notch or a pin one identification mark shall be located ed adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
- The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
- Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
- Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
- This dimension allows for off-center lid, meniscus, and glass overrun
- Dimension Q shall be measured from the seating plane to the base plane.
- 7. Measure dimension S1 at all four corners.
- 8. N is the maximum number of terminal positions.
- 9. Dimensioning and tolerancing per ANSI Y14.5M 1982.
- 10. Controlling dimension: INCH.

F24.6 MIL-STD-1835 GDIP1-T24 (D-3, CONFIGURATION A) 24 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

1 1	INC	HES	MILLIM	ETERS	
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
С	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.290		32.77	5
Ε	0.500	0.610	12.70	15.49	5
е	0.100	BSC	2.54 BSC		-
eA	0.600	BSC	15.24 BSC		-
eA/2	0.300	BSC	7.62 BSC		-
L	0.120	0.200	3.05	5.08	-
Q	0.015	0.075	0.38	1.91	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
М	-	0.0015	-	0.038	2,3
N	2	4	2	4	8

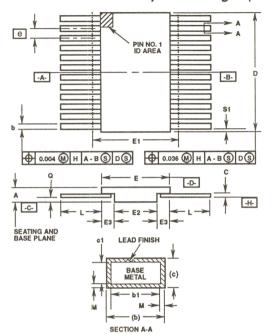
Rev. 0 4/94

F20.3 MIL-STD-1835 GDIP1-T20 (D-8, CONFIGURATION A) 20 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
С	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D		1.060	-	26.92	5
E	0.220	0.310	5.59	7.87	5
е	0.100 BSC		2.54 BSC		-
eA	0.300	BSC	7.62 BSC		
eA/2	0.150	BSC	3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
М	-	0.0015	-	0.038	2, 3
N	2	0	2	0	8

Rev. 0 4/94

Ceramic Metal Seal Flatpack Packages (Flatpack)



NOTES:

- Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
- 2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
- This dimension allows for off-center lid, meniscus, and glass overrun.
- 4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
- 5. N is the maximum number of terminal positions.
- 6. Measure dimension S1 at all four corners.
- For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
- Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
- 9. Dimensioning and tolerancing per ANSI Y14.5M 1982.
- 10. Controlling dimension: INCH.

K14.B
14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

	INCI	HES	MILLIM	ETERS	
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
С	0.003	0.009	0.08	0.23	-
c1	0.003	0.007	0.08	0.18	-
D	-	0.390	-	9.91	3
E	0.235	0.260	5.97	6.60	-
E1	-	0.290	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76		7
е	0.050	BSC	1.27	BSC	-
k	0.008	0.015	0.20	0.38	2
L	0.270	0.370	6.86	9.40	-
Q	0.010	0.020	0.25	0.51	8
S1	0.005	-	0.13	-	6
М	-	0.0015	-	0.04	-
N	1	4	1	4	-

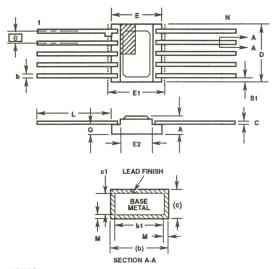
Rev. 0 6/14/94

K16.D
16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

	INC	HES	MILLIM	ETERS	
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
С	0.003	0.009	0.08	0.23	-
c1	0.003	0.007	0.08	0.18	-
D	-	0.440	-	11.18	3
E	0.245	0.285	6.22	7.24	-
E1	-	0.315	-	8.00	3
E2	0.130	-	3.30	-	-
E3	0.030	-	0.76	-	7
е	0.050	BSC	1.27	BSC	-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.010	0.020	0.25	0.51	8
S1	0.000	-	0.00	-	6
М	-	0.0015		0.04	-
N	1	6	1	6	-
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Rev. 0 6/14/94

Ceramic Metal Seal Flatpack Packages (Flatpack) (Continued)



NOTES:

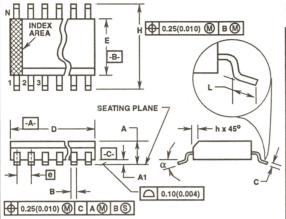
- Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
- If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
- 3. This dimension allows for off-center lid, meniscus, and glass
- 4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
- 5. N is the maximum number of terminal positions.
- 6. Measure dimension S1 at all four corners.
- For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
- Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
- 9. Dimensioning and tolerancing per ANSI Y14.5M 1982.
- 10. Controlling dimension: INCH.
- 11. The basic lead spacing is 0.050 inch (1.27mm) between center lines. Each lead centerline shall be located within ±0.005 inch (0.13mm) of its exact longitudinal position relative to lead 1 and the highest numbered (N) lead.

K24.D TOP BRAZED 24 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

	INC	HES	MILLIM	ETERS	
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	0.045	0.115	1.14	2.92	-
b	0.017	0.025	0.43	0.64	-
b1	0.017	0.022	0.43	0.56	-
С	0.003	0.010	0.08	0.26	-
c1	0.003	0.007	0.08	0.18	-
D	-	0.720	-	18.29	-
Е	0.630	0.650	16.00	16.51	-
E1	-	0.680	-	17.27	3
E2	0.530	-	13.46	-	-
е	0.050	BSC	1.27	BSC	-
k	-	-		-	-
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.050	0.66	1.27	-
S1	0.000	-	0.000	-	-
М	-	0.0015	-	0.04	-
N	2	4	2	4	-

Rev. 0 6/17/94

Small Outline Plastic Packages (SOIC)



NOTES:

- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
- 2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
- Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
- The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
- 6. "L" is the length of terminal for soldering to a substrate.
- 7. "N" is the number of terminal positions.
- 8. Terminal numbers are shown for reference only.
- The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
- Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M14.15 (JEDEC MS-012-AB ISSUE C)
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

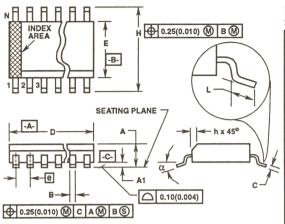
	INC	HES	MILLIM	ETERS	
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
В	0.013	0.020	0.33	0.51	9
С	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
е	0.050	BSC	1.27	BSC	-
Н	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	1	4	1	4	7
α	0°	8°	0°	8°	-

Rev. 0 12/93

M16.15 (JEDEC MS-012-AC ISSUE C) 16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

	INC	HES	MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
В	0.013	0.020	0.33	0.51	9
С	0.0075	0.0098	0.19	0.25	
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
е	0.050	BSC	1.27	BSC	-
Н	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	1	6	1	6	7
α	0°	8°	0°	8°	·

Small Outline Plastic Packages (SOIC) (Continued)



NOTES:

- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
- 2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
- Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
- 5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
- 6. "L" is the length of terminal for soldering to a substrate.
- 7. "N" is the number of terminal positions.
- 8. Terminal numbers are shown for reference only.
- The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
- Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

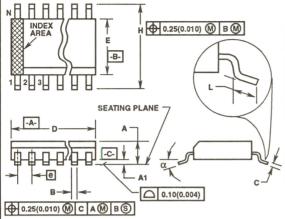
	INC	HES	MILLIM	ETERS	
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
В	0.013	0.0200	0.33	0.51	9
С	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
е	0.050	BSC	1.27	BSC	-
Н	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		2	.0	7
α	0°	8°	0°	8°	-

Rev. 0 12/93

M24.3 (JEDEC MS-013-AD ISSUE C)
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

	INC	HES	MILLIM	ETERS	
SYMBOL	MIN	MAX	MIN	MAX	NOTES
А	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
В	0.013	0.020	0.33	0.51	9
С	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
е	0.05	BSC	1.27	BSC	-
Н	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		2	24	7
α	0°	8°	0°	8°	-

Shrink Small Outline Plastic Packages (SSOP)



M16.209 (JEDEC MO-150-AC ISSUE A) 16 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

	INC	HES	MILLIM	ETERS	
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	-	0.083	-	2.13	-
A1	0.002	0.009	0.05	0.25	-
В	0.009	0.014	0.22	0.38	9
С	0.004	0.007	0.09	0.20	
D	0.233	0.255	5.90	6.50	3
Е	0.197	0.220	5.00	5.60	4
е	0.026	BSC	0.65	BSC	
Н	0.292	0.322	7.40	8.20	
L	0.025	0.040	0.63	1.03	6
N	16		1	6	7
α	0°	8°	0°	8°	-

Rev. 1 6/94

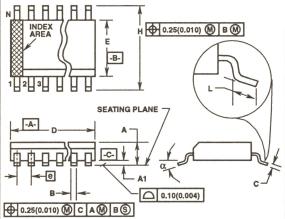
NOTES:

- 1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
- 2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
- Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
- 5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
- 6. "L" is the length of terminal for soldering to a substrate.
- 7. "N" is the number of terminal positions.
- 8. Terminal numbers are shown for reference only.
- The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.51mm (0.020 inch)
- Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M20.209 (JEDEC MO-150-AE ISSUE A) 20 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

	INC	HES	MILLIM	ETERS	
SYMBOL	MIN	MAX	MIN	MAX	NOTES
Α	-	0.083	-	2.13	-
A1	0.002	0.009	0.05	0.25	-
В	0.009	0.014	0.22	0.38	9
С	0.004	0.007	0.09	0.20	-
D	0.272	0.295	6.90	7.50	3
Е	0.197	0.220	5.00	5.60	4
е	0.026	BSC	0.65	BSC	-
Н	0.292	0.322	7.40	8.20	-
L	0.025	0.040	0.63	1.03	6
N	20		2	0	7
α	0°	8°	0°	8°	-

Shrink Small Outline Plastic Packages (SSOP) (Continued)



M24.209 (JEDEC MO-150-AG ISSUE A)
24 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

	INCHES		MILLIM	ETERS	
SYMBOL	MIN	MAX	MIN	MAX	NOTES
А	-	0.083	-	2.13	-
A1	0.002	0.009	0.05	0.25	-
В	0.009	0.014	0.22	0.38	9
С	0.004	0.007	0.09	0.20	-
D	0.312	0.334	7.90	8.50	3
E	0.197	0.220	5.00	5.60	4
ө	0.026	BSC	0.65	BSC	-
Н	0.292	0.322	7.40	8.20	-
L	0.025	0.040	0.63	1.03	6
N	24		2	4	7
α	0°	8°	0°	8°	-

Rev. 0 6/94

NOTES:

- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
- 2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
- Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
- The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
- 6. "L" is the length of terminal for soldering to a substrate.
- 7. "N" is the number of terminal positions.
- 8. Terminal numbers are shown for reference only.
- The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.51mm (0.020 inch)
- Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

CMOS LOGIC ICs

8

PRODUCT SELECTION GUIDE

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/	PUB. NUMBER	DATA BOOK/DESCRIPTION
	SG103	CMOS LOGIC SELECTION GUIDE (1994: 288pp) This product selection guide contains technical information on Harri Semiconductor High Speed 54/74 CMOS Logic Integrated Circuits for commercial, industrial and military applications. covers Harris' High Speed CMOS Logic HC/HCT Series, AC/ACT Series, BiCMOS Interface Logic FCT Series and CMO Logic CD4000B Series.
	PSG201.21	PRODUCT SELECTION GUIDE (NEW 1994: 616pp) Key product information on all Harris Semiconductor devices Sectioned (Linear, Data Acquisition, Digital Signal Processing, Telecom, Intelligent Power, Discrete Power, Digital Microprocessors and Hi-Rel/Military and Rad Hard) for easy use and includes cross references and alphanumeric panumber index.
	DB500B	LINEAR AND TELECOM ICs (1993: 1,312pp) Product specifications for: op amps, comparators, S/H amps, differentia amps, arrays, special analog circuits, telecom ICs, and power processing circuits.
	DB301B	DATA ACQUISITION (1994: 1,104pp) Product specifications on A/D converters (display, integrating, successive approximation, flash); D/A converters, switches, multiplexers, and other products.
	DB302B	DIGITAL SIGNAL PROCESSING (1994: 528pp) Product specifications on one-dimensional and two-dimensional filter signal synthesizers, multipliers, special function devices (such as address sequencers, binary correlators, histogrammer).
	DB304.1	INTELLIGENT POWER ICs (1994: 946pp) This data book includes a complete set of data sheets for product specification: application notes with design details for specific applications of Harris products, and a description of the Harris quality an high reliability program.
	DB450.4	TRANSIENT VOLTAGE SUPPRESSION DEVICES (1995: 400pp) Product specifications of Harris varistors and surgector Also, general informational chapters such as: "Voltage Transients - An Overview," "Transient Suppression - Devices ar Principles," "Suppression - Automotive Transients."
	DB223B	POWER MOSFETs (1994: 1,328pp) This data book contains detailed technical information including standard pown MOSFETs (the popular RF-series types, the IRF-series of industry replacement types, and JEDEC types), MegaFETs, logical level power MOSFETs (L ² FETs), ruggedized power MOSFETs, advanced discrete, high-reliability and radiation-hardened power MOSFETs.
	DB235B	RADIATION HARDENED (1993: 2,232pp) Harris technologies used include dielectric isolation (DI), Silicon-on-Sapphii (SOS), and Silicon-on-Insulator (SOI). The Harris radiation-hardened products include the CD4000, HCS/HCTS and ACTS logic families, SRAMs, PROMs, op amps, analog multiplexers, the 80C85/80C86 microprocessor family, analog witches, gate arrays, standard cells and custom devices.
	DB260.2	CDP6805 CMOS MICROCONTROLLERS & PERIPHERALS (1995: 436pp) This data book represents the full line of Harr Semiconductor CDP6805 products for commercial applications and supersedes previously published CDP6805 data book under the Harris, GE, RCA or Intersil names.
	DB303	MICROPROCESSOR PRODUCTS (1992: 1,156pp) For commercial and military applications. Product specifications of CMOS microprocessors, peripherals, data communications, and memory ICs.
	DB309.1	MCT/IGBT/DIODES (1995: est 700pp) This MCT/IGBT/Diodes Databook represents the full line of these products made the Harris Semiconductor Discrete Power Products for commercial applications.
	Analog Military	ANALOG MILITARY (1989: 1,264pp) This data book describes Harris' military line of Linear, Data Acquisition, ar Telecommunications circuits.
	DB312	ANALOG MILITARY DATA BOOK SUPPLEMENT (1994: 432pp) The 1994 Military Data Book Supplement, combined withe 1989 Analog Military Product Data Book, contain detailed technical information on the extensive line of Harr Semiconductor Linear and Data Acquisition products for Military (MIL-STD-883, DESC SMD and JAN) applications are supersedes all previously published Linear and Data Acquisition Military data books. For applications requiring Radiation Hardened products, please refer to the 1993 Harris Radiation Hardened Product Data Book (document #DB235B)
	Digital Military	DIGITAL MILITARY (1989: 680pp) Harris CMOS digital ICs – microprocessors, peripherals, data communications ar memory – are included in this data book.
	7004	Complete Set of Commercial Harris Data Books
٦	7005	Complete Set of Commercial and Military Harris Data Books

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AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
27007	BR007	Complete Listing of Harris Sales Offices, Representatives and Authorized Distributors World Wide (7 pages)
LOGIC PACK	AGING INFORMATION	V
7020	SG103 Section 7	Logic Packaging Information (15 pages)
CD4000B SEI	RIES LOGIC DATA SH	EETS
7012	CMOS Logic ICs - CD4000B Series	Harris' High-Reliability CD4000B Series of high-voltage CMOS ICs consists of a broad range of SSI, MSI-1, and MSI-2 (LSI) functions from simple gates to complex counters, registers, and arithmetic circuits. (38 pages)
CD4000 SERI	ES LOGIC DATA SHE	ETS
985	CD4001B, CD4002B, CD4025B Types	CMOS NOR Gates (4 pages)
945	CD4001UB Types	CMOS Quad 2-Input NOR Gate (3 pages)
1033	CD4006B Types	CMOS 18-Stage Static Shift Register (4 pages)
977	CD4007UB Types	CMOS Dual Complementary Pair Plus Inverter (4 pages)
951	CD4008B Types	CMOS 4-Bit Full Adder (4 pages)
940	CD4009UB, CD4010B Types	CMOS Hex Buffers/Converters (4 pages)
3718	CD4011B, CD4012B, CD4023B Types	CMOS NAND Gates (4 pages)
947	CD4011UB Types	CMOS Quad 2-Input NAND Gate (3 pages)
936	CD4013B Types	CMOS Dual 'D'-Type Flip-Flop (4 pages)
1043	CD4014B, CD4021B Types	CMOS 8-Stage Static Shift Registers (5 pages)
1024	CD4015B Types	CMOS Dual 4-Stage Static Shift Register (4 pages)
953	CD4016B Types	CMOS Quad Bilateral Switch (5 pages)
1113	CD4017B, CD4022B Types	CMOS Counter/Dividers (6 pages)
1034	CD4018B Types	CMOS Presettable Divide-By- "N" Counter (5 pages)
1045	CD4019B Types	CMOS Quad AND/OR Select Gate (4 pages)

AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
1063	CD4020B, CD4024B, CD4040B Types	CMOS Ripple-Carry Binary Counter/Dividers (4 pages)
1118	CD4026B, CD4033B Types	CMOS Decade Counters/ Dividers (6 pages)
942	CD4027B Types	CMOS Dual J-K Master-Slave Flip-Flop (4 pages)
1016	CD4028B Types	BCD-to-Decimal Decoder (4 pages)
1028	CD4029B Types	CMOS Presettable Up/Down Counter (6 pages)
1055	CD4030B Types	CMOS Quad Exclusive-OR Gate (3 pages)
1073	CD4031B Types	CMOS 64-Stage Static Shift Register (5 pages)
1062	CD4034B Types	CMOS 8-Stage Static Bidirectional Parallel/Serial Input/Output Bus Register (6 pages)
1101	CD4035B Types	CMOS 4-Stage Parallel In/ Parallel Out Shift Register (5 pages)
934	CD4041UB Types	CMOS Quad True/ Complement Buffer (3 pages)
954	CD4042B Types	CMOS Quad Clocked "D" Latch (4 pages)
956	CD4043B, CD4044B Types	CMOS Quad 3-State R/S Latches (4 pages)
1119	CD4045B Types	CMOS 21-Stage Counter (4 pages)
1099	CD4046B Types	CMOS Micropower Phase- Locked Loop (6 pages)
1123	CD4047B Types	CMOS Low-Power Monostable/Astable Multivibrator (7 pages)
1124	CD4048B Types	CMOS Multifunction Expandable 8-Input Gate (5 pages)
926	CD4049UB, CD4050B Types	CMOS Hex Buffer/Converters (4 pages)
902	CD4051B, CD4052B, CD4053B Types	CMOS Analog Miltiplexers/ Demultiplexers (7 pages)
634	CD4054B, CD4055B, CD4056B Types	CMOS Liquid-Crystal Display Drivers (5 pages)
898	CD4059A Types	CMOS Programmable Divide- by-"N" Counter (8 pages)

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AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
1120	CD4060B Types	CMOS 14-Stage Ripple-Carry Binary Counter/Divider and Oscillator (4 pages)
805	CD4063B Types	CMOS 4-Bit Magnitude Comparator (4 pages)
1114	CD4066B Types	CMOS Quad Bilateral Switch (5 pages)
3719	CD4067B, CD4097B Types	CMOS Analog Multiplexers/ Demultiplexers (6 pages)
809	CD4068B Types	CMOS 8-Input NAND/AND Gate (3 pages)
804	CD4069UB Types	CMOS Hex Inverter (3 pages)
910	CD4070B, CD4077B Types	CMOS Quad Exclusive-OR and Exlusive-NOR Gates (3 pages)
807	CD4071B, CD4072B, CD4075B Types	CMOS or Gates (4 pages)
806	CD4073B, CD4081B, CD4082B Types	CMOS AND Gates (4 pages)
903	CD4076B Types	CMOS 4-Bit D-Type Registers (4 pages)
810	CD4078B Types	CMOS 8-Input NOR/OR Gate (3 pages)
811	CD4085B Types	CMOS Dual 2-Wide 2-Input AND-OR-INVERT Gate (4 pages)
812	CD4086B Types	CMOS Expandable 4-Wide 2-Input AND-OR-INVERT Gate (4 pages)
1003	CD4089B Types	CMOS Binary Rate Multiplier (5 pages)
836	CD4093B Types	CMOS Quad 2-Input NAND Schmitt Triggers (4 pages)
3707	CD4094B Types	CMOS 8-Stage Shift-and-Store Bus Register (4 pages)
879	CD4095B, CD4096B Types	CMOS Gated J-K Master- Slave Flip-Flops (4 pages)
979	CD4098B Types	CMOS Dual Monostable Multivibrator (5 pages)
948	CD4099B Types	CMOS 8-Bit Addressable Latch (4 pages)
1002	CD4502B Types	CMOS Strobed Hex Inverter/ Buffer (3 pages)
1224	CD4503B Types	CMOS Hex Buffer (3 pages)
1846	CD4504B Types	CMOS Hex Voltage-Level Shifter for TTL-to-CMOS or CMOS-to-CMOS Operation (4 pages)

AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
1009	CD4508B Types	CMOS Dual 4-Bit Latch (4 pages)
899	CD4510B, CD4516B Types	CMOS Presettable Up/Down Counters (6 pages)
901	CD4511B Types	CMOS BCD-to-7-Segment Latch Decoder Drivers (5 pages)
1032	CD4512B Types	CMOS 8-Channel Data Selector (3 pages)
3721	CD4514B, CD4515B Types	CMOS 4-Bit Latch/4-to-16 Line Decoders (4 pages)
1148	CD4517B Types	CMOS Dual 64-Stage Static Shift Register (5 pages)
808	CD4518B, CD4520B Types	CMOS Dual Up-Counters (5 pages)
1723	CD4519B Types	CMOS 4-Bit AND/OR Selector, Quad 2-Channel Data Selector, or Quad Exclusive NOR Gate (5 pages)
1735	CD4521B Types	CMOS 24-Stage Frequency Drivider (7 pages)
1710	CD4522B Types	CMOS Programmable BCD Divide-by-"N" Counter (7 pages)
1006	CD4527B Types	CMOS BCD Rate Multiplier (5 pages)
1720	CD4529B Types	CMOS Dual 4-Channel Analog Data Selector (6 pages)
876	CD4532B Types	CMOS 8-Bit Priority Encoder (4 pages)
1186	CD4536B Types	CMOS Programmable Timer High-Voltage Types (20V Rating) (8 pages)
1245	CD4538B Types	CMOS Dual Precision Monostable Multivibrator (1 pages) Obsolete - See Part Number CD14538B, AnswerFAX Document Number 3737
1378	CD4541B Types	CMOS Programmable Timer High-Voltage Types (20V Rating) (4 pages)
1327	CD4543B Types	CMOS BCD-to-Seven- Segment Latch/Decoder/ Driver for Liquid-Crystal Displays (6 pages)
858	CD4555B, CD4556B Types	CMOS Dual Binary to 1 of 4 Decoder/Demultiplexers (5 pages)
1711	CD4560B Types	CMOS NBCD Adder (5 pages)



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DOCUMENT	PART	
NUMBER	NUMBER	DESCRIPTION
1728	CD4566B Types	CMOS Industrial Timer-Base
		Generator High-Voltage Types (20V Rating) (6 pages)
1704	CD4572UB Types	CMOS Hex Gate (5 pages)
1146	CD4585B Types	CMOS 4-Bit Magnitude Comparator (4 pages)
1111	CD4724B	CMOS 8-Bit Addressable Latch (4 pages)
1725	CD7211, CD7211A Types	CMOS Four-Digit LCD Decoders-Drivers (5 pages)
1726	CD7211M, CD72211AM Types	CMOS Four-Digit LCD Decoders-Drivers (5 pages)
3737	CD14538B Types	CMOS Dual Precision Monostable Multivibrator (7 pages)
1686	CD22402	Sync Generator for TV Applications and Video Processing Systems (10 pages)
1869	CD22777 Types	CMOS 32kHz Quartz Analog Clock Circuit (4 pages)
980	CD40100B Types	CMOS 32-Stage Static Left/ Right Shift Register (5 pages)
984	CD40102B, CD40103B Types	CMOS 8-Stage Presettable Synchronous Down Counters (7 pages)
1044	CD40105B Types	CMOS FIFO Register (5 pages)
1017	CD40106B Types	CMOS Hex Schmitt Triggers (4 pages)
1015	CD40107B	CMOS Dual 2-Input NAND Buffer/Driver (3 pages)
3722	CD40109B Types	CMOS Quad Low-to-High Voltage Level Shifter (4 pages)
1125	CD40110B Types	CMOS Decade Up-Down Counter/Latch/Display Driver (9 pages)
1234	CD40116 Types	CMOS High-Speed 8-Bit Bidirectional CMOS/TTL Interface Level Converter (6 pages)
1333	CD40117B Types	Programmable Dual 4-Bit Terminator (4 pages)
1117	CD40147B Types	10-Line to 4-Line BCD Priority Encoder (3 pages)
1047	CD40160B, CD40161B, CD40163B Types	CMOS Synchronous PRogrammable 4-Bit Counters (7 pages)
1031	CD40174B Types	CMOS Hex 'D'-Type Flip-Flop (4 pages)

AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
1326	CD40175B Types	CMOS Quad 'D'-Type Flip- Flop (6 pages)
993	CD40192B, CD40193B Types	CMOS Presettable Up/Down Counters (Dual Clock with Reset) (5 pages)
1220	CD40194B	CMOS 4-Bit Bidirectional Universal Shift Register (6 pages)
982	CD40257B	CMOS Quad 2-Line-to-1-Line Data Selector/Multiplexer (3 pages)
CD54/74 AC/	ACT COMMERCIAL L	OGIC DATA SHEETS
1855	CD54/74AC00, CD54/74ACT00	Quad 2-Input NAND Gate (4 pages)
1978	CD54/74AC02, CD54/74ACT02	Quad 2-Input NOR Gate (4 pages)
1945	CD54/74AC04, CD54/74AC05, CD54/74ACT04, CD54/74ACT05	Hex Inverters (4 pages)
1950	CD54/74AC08, CD54/74ACT08	Quad 2-Input AND Gate (4 pages)
1977	CD54/74AC10, CD54/74ACT10	Triple 3-Input NAND Gate (5 pages)
1984	CD54/74AC14, CD54/74ACT14	Hex Inverting Schmitt Trigger (5 pages)
1976	CD54/74AC20, CD54/74ACT20	Dual 4-Input NAND Gate (5 pages)
1951	CD54/74AC32, CD54/74ACT32	Quad 2-Input OR Gate (4 pages)
1881	CD54/74AC74, CD54/74ACT74	Dual D-Type Flip-Flop with Se and Reset Positive-Edge- Triggered (6 pages)
1952	CD54/74AC86, CD54/74ACT86	Qual 2-Input Exclusive-OR Gate (4 pages)
1967	CD54/74AC109, CD54/74AC112, CD54/74ACT109, CD54/74ACT112	Dual "J-K" Flip-Flop With Set and Reset (7 pages)
1909	CD54/74AC138, CD54/74AC238, CD54/74ACT138, CD54/74ACT238	3-to-8-Line Decoders/ Demultiplexers AC/ACT138- Inverting AC/ACT238 - Non- Inverting (6 pages)
1953	CD54/74AC139, CD54/74ACT139	Dual 2-to-4-Line Decoder/ Demultiplexer (5 pages)
1980	CD54/74AC151, CD54/74ACT151	8-Input Multiplexer (6 pages)
1966	CD54/74AC153, CD54/74ACT153	Dual 4-Input Multiplexer (6 pages)



AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
1910	CD54/74AC157, CD54/74AC158, CD54/ACT157, CD54/74ACT158	Quad 2-Input Multiplexers (6 pages)
1959	CD54/74AC161, CD54/74AC163, CD54/74ACT161, CD54/74ACT163	Synchronous Presettable Binary Counters (9 pages)
1954	CD54/74AC164, CD54/74ACT164	8-Bit Serial-In/Parallel-Out Shift Register (6 pages)
1973	CD54/74AC174, CD54/74ACT174	Hex D Flip-Flop with Reset (6 pages)
1964	CD54/74AC175, CD54/74ACT175	Quad D Flip-Flop with Reset (6 pages)
1911	CD54/74AC191, CD54/74ACT191	Presettable Synchronous 4-Bit Binary Up/Down Counter (9 pages)
1947	CD54/74AC193, CD54/74ACT193	Presettable Synchronous 4-Bit Binary Up/Down Counter with Reset (9 pages)
1856	CD54/74AC240, CD54/74AC241, CD54/74AC244, CD54/74ACT240, CD54/74ACT241, CD54/74ACT244	Octal Buffer/Line Drivers, 3- State (6 pages)
1907	CD54/74AC245, CD54/74ACT245	Octal-Bus Tranceiver, 3-State, Non-Inverting (6 pages)
1981	CD54/74AC251, CD54/74ACT251	8-Input Multiplexer, 3-State (6 pages)
1985	CD54/74AC253, CD54/74ACT253	Dual 4-Input Multiplexer, 3-State (6 pages)
1955	CD54/74AC257, CD54/74AC258, CD54/74ACT257, CD54/74ACT258	Qual 2-Input Multiplexer with 3-State Outputs (6 pages)
1979	CD54/74AC273, CD54/74ACT273	Octal D Flip-Flop with Reset (6 pages)
1957	CD54/74AC280, CD54/74ACT280	9-Bit Odd/Even Parity Generator/Checker (4 pages)
1912	CD54/74AC283, CD54/74ACT283	4-Bit Binary Full Adder with Fast Carry (4 pages)
2195	CD54/74AC297, CD54/74ACT297	Digital Phase-Locked Group (7 pages)
1958	CD54/74AC299, CD54/74AC323, CD54/74ACT299, CD54/74ACT323	8-Input Universal Shift/Storage Register with Common Parallel I/O Pins (9 pages)
1882	CD54/74AC373, CD54/74AC533, CD54/74ACT373, CD54/74ACT533	Octal Transparent Latch, 3-State (7 pages)

AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
1883	CD54/74AC374, CD54/74AC534, CD54/74ACT374, CD54/74ACT534	Octal D-Type Flip-Flops, 3-State Positive-Edge Triggered (7 pages)
1857	CD54/74AC540, CD54/74AC541, CD54/74ACT540, CD54/74ACT541	Octal Buffer/Line Drivers, 3-State (6 pages)
1956	CD54/74AC563, CD54/74AC573, CD54/74ACT563, CD54/74ACT573	Octal Transparent Latch, 3-State (7 pages)
1948	CD54/74AC564, CD54/74AC574, CD54/74ACT564, CD54/74ACT574	Octal D-Type Flip-Flop, 3-State Positive-Edge-Triggered (7 pages)
1968	CD54/74AC623, CD54/74ACT623	Octal-Bus Transceiver, 3-State, Non-Inverting (6 pages)
1970	CD54/74AC646, CD54/74AC648, CD54/74ACT646, CD54/74ACT648	Octal-Bus Transceiver/ Registers, 3-State (7 pages)
1982	CD54/74AC647, CD54/74ACT647,	Octal-Bus Transceiver/ Registers, with Open Drain Non-Inverting (7 pages)
1974	CD54/74AC651, CD54/74AC652, CD54/74ACT651, CD54/74ACT652	Octal-Bus Transceiver/ Registers, 3-State (7 pages)
1975	CD54/74AC653, CD54/74AC654, CD54/74ACT653, CD54/74ACT654	Octal-Bus Transceivers/ Registers, Open-Drain (A Side), 3-State (B Side) (8 pages)
2062	CD54/74AC7060, CD54/74AC7061, CD54/74ACT7060, CD54/74ACT7061	14-Stage Binary Counter with Oscillator (6 pages)
1969	CD54/74AC7623, CD54/74ACT7623	Octal-Bus Transceiver, 3-State (B Side), Open Drain (A Side), Non-Inverting (6 pages)
CD54 AC/AC	THI-REL LOGIC DATA	SHEETS
3876	CD54AC00/3A, CD54ACT00/3A	Quad 2-Input NAND Gate (1 pages)
3877	CD54AC02/3A, CD54ACT02/3A	Quad 2-Input NOR Gate (1 pages)
3878	CD54AC04/3A, CD54ACT04/3A	Hex Inverters, Active Outputs (1 pages)
3879	CD54AC05/3A, CD54ACT05/3A	Hex Inverters, Open-Drain Outputs (1 pages)





AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
3880	CD54AC08/3A, CD54ACT08/3A	Quad 2-Input AND Gate (1 pages)
3881	CD54ACT20/3A	Dual 4-Input NAND Gate (1 pages)
3882	CD54AC32/3A, CD54ACT32/3A	Quad 2-Input OR Gate (1 pages)
3883	CD54AC74/3A, CD54ACT74/3A	Dual D-Type Flip-Flop with Set and Reset (1 pages)
3884	CD54ACT86/3A	Quad 2-Input Exclusive-OR Gate (1 pages)
3885	CD54AC109/3A, CD54ACT109/3A	Dual "J-K" Flip-Flop with Set and Reset (1 pages)
3886	CD54AC112/3A, CD54ACT112/3A	Dual "J-K" Flip-Flop with Set and Reset (1 pages)
3887	CD54AC138/3A, CD54ACT138/3A	3-to-8-Line Decoder/Demulti- plexer Inverting (1 pages)
3888	CD54AC139/3A, CD54ACT139/3A	Dual 2-to-4-Line Decoder/ Demultiplexer (1 pages)
3889	CD54ACT151/3A	8-Input Multiplexer (1 pages)
3890	CD54AC153/3A, CD54ACT153/3A	Dual 4-Input Multiplexer (1 pages)
3891	CD54AC157/3A	Quad 2-Input Multiplexer Non- Inverting (1 pages)
3892	CD54AC161/3A, CD54ACT161/3A	Synchronous Presettable Binary Counters (1 pages)
3893	CD54AC163/3A, CD54ACT163/3A	Synchronous Presettable Binary Counters (1 pages)
3894	CD54AC164/3A, CD54ACT164/3A	8-Bit Serial-In/Parallel-Out Shift Registers (1 pages)
3895	CD54ACT174/3A	Hex D Flip-Flop with Reset (1 pages)
3896	CD54AC191/3A, CD54ACT191/3A	Presettable Synchronous 4-Bit Binary Up/Down Counters (1 pages)
3897	CD54AC193/3A, CD54ACT193/3A	Presettable Synchronous 4-Bit Binary Up/Down Counter with Reset (1 pages)
3898	CD54AC240/3A, CD54ACT240/3A	Octal Buffer/Line Driver Three- State, Inverting (1 pages)
3899	CD54ACT241/3A	Octal-Buffer/Line Driver, Three-State (1 pages)
3900	CD54AC244/3A, CD54ACT244/3A	Octal Buffer/Line Driver Three- State, Non-Inverting (1 pages)
3901	CD54AC245/3A, CD54ACT245/3A	Octal-Bus Transceiver Three- State, Non-Inverting (1 pages)
3902	CD54ACT253/3A	Dual 4-Input Multiplexer, Three-State (1 pages)

AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	
3903	CD54AC257/3A, CD54ACT257/3A	Quad 2-Input Multiplexer Three-State, Non-Inverting (1 pages)	
3904	CD54AC273/3A, CD54ACT273/3A	Octal D Flip-Flop with Reset (1 pages)	
3905	CD54AC280/3A, CD54ACT280/3A	9-Bit Odd/Even Parity Generator/Checker (1 pages)	
3906	CD54AC283/3A, CD54ACT283/3A	4-Bit Binary Full Adder with Fast Carry (1 pages)	
3907	CD54AC299/3A, CD54ACT299/3A	8-Input Universal Shift/Storage Registers with Common Paral- lel I/O Pins (2 pages)	
3908	CD54ACT323/3A	8-Input Universal Shift/Storage Register with Common Parallel I/O Pins (2 pages)	
3909	CD54AC373/3A, CD54ACT373/3A	Octal Transparent Latch Three-State, Non-Inverting (1 pages)	
3910	CD54AC374/3A, CD54ACT374/3A	Octal D-Type Flip-Flop, Three- State Positive-Edge Triggered, Non-Inverting (1 pages)	
3911	CD54ACT533/3A	Octal Transparent Latch, Three-State, Inverting (1 pages)	
3912	CD54AC534/3A, CD54ACT534/3A	Octal D-Type Flip-Flop, Three- State Positive-Edge Triggered, Inverting (1 pages)	
3913	CD54ACT540/3A	Octal Buffer/Line Driver, Three-State, Inverting (1 pages)	
3914	CD54AC541/3A, CD54ACT541/3A	Octal Buffer/Line Driver Three- State, Non-Inverting (1 pages)	
3915	CD54AC573/3A, CD54ACT573/3A	Octal Transparent Latch Three-State, Non-Inverting (1 pages)	
3916	CD54AC574/3A, CD54ACT574/3A	Octal D-Type Flip-Flop, Three- State Positive-Edge Triggered, Non-Inverting (1 pages)	
3917	CD54ACT623/3A	Octal Bus Transceiver Three- State, Non-Inverting (1 pages)	
CD54/74 FC1	CD54/74 FCT LOGIC DATA SHEETS		
2227	CD54/74FCT240, CD54/74FCT240AT, CD54/74FCT241, CD54/74FCT244, CD54/74FCT244AT	Octal Buffers/Line Drivers, 3-State (5 pages)	
2301	CD54/74FCT245, CD5474FCT245AT	Octal-Bus Transceiver, 3-State, Non-Inverting (5 pages)	
2303	CD54/74FCT273	Octal D Flip-Flop with Reset (4 pages)	

HOW TO USE ANSWERFAX

AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
2230	CD54/74FCT373, CD54/74FCT373AT, CD54/74FCT533	Octal Transparent Latch, 3-State (5 pages)
2305	CD54/74FCT374, CD54/74FCT374AT	Octal D-Type Flip-Flops, 3-State Positive-Edge Triggered (5 pages)
2383	CD54/74FCT540, CD54/74FCT541	Octal Buffers/Line Drivers, 3-State (5 pages)
2399	CD54/74FCT543	Octal Register-Transceivers, 3-State (5 pages)
2295	CD54/74FCT564, CD54/74FCT574, CD54/74FCT574AT	Octal D-Type Flip-Flops, 3-State Positive-Edge Triggered(5 pages)
2304	CD54/74FCT573, CD54/74FCT573AT	Octal Transparent Latch, 3-State (5 pages)
2302	CD54/74FCT623	Octal Bus Transceiver, 3-State Non-Inverting (5 pages)
2393	CD54/74FCT646, CD54/74FCT646AT	Octal Bus Transceivers/ Registers, 3-State (5 pages)
2394	CD54/74FCT651, CD54/74FCT652	Octal Bus Transceivers/ Registers, 3-State (5 pages)
2403	CD54/74FCT653, CD54/74FCT654	Octal Bus Transceivers/ Registers, Open-Drain (A Side), 3-State (B Side) (6 pages)
2390	CD54/74FCT821A, CD54/74FCT822A	10-Bit D-Type Flip-Flops, 3-State, Positive-Edge Triggered (5 pages)
2389	CD54/74FCT823A, CD54/74FCT824A	9-Bit D-Type Flip-Flops, 3-State, Positive-Edge- Triggered (5 pages)
2397	CD54/74FCT841A, CD54/74FCT842A	10-Bit Transparent Latch, 3-State (5 pages)
2396	CD54/74FCT843A, CD54/74FCT844A	9-Bit Transparent Latch, 3-State (5 pages)
2392	CD54/74FCT861A	10-Bit Bus Transceivers, 3-State (5 pages)
2391	CD54/74FCT863A	9-Bit Bus Transceivers, 3-State (5 pages)
2400	CD54/74FCT2952A	Octal Register-Transceivers, 3-State (5 pages)
2358	CD54/74FCT7623	Octal Bus Transceiver, 3-State, (B Side), Open-Drain (A Side), Non-Inverting (5 pages)
2196	CD54/74FCT7651	Octal Bus Transceiver/Register, 3-State, Inverting (1 pages) Obsolete - See Part Number CD74ACT651, AnswerFAX Document Number 1974

AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
CD54/74 HC/F	HCT COMMERCIAL I	LOGIC DATA SHEETS
1464	CD54/74HC00, CD54/74HCT00	High-Speed CMOS Logic, Quad 2-Input NAND Gate (4 pages)
1647	CD54/74HC02, CD54/74HCT02	High-Speed CMOS Logic, Quad 2-Input NOR Gate (4 pages)
1832	CD54/74HC03, CD54/74HCT03	High-Speed CMOS Logic, Quad 2-Input NAND Gate with Open Drain (4 pages)
1471	CD54/74HC04, CD54/74HCT04	High-Speed CMOS Logic, He Inverter (4 pages)
1549	CD54/74HC08, CD54/74HCT08	High-Speed CMOS Logic, Quad 2-Input AND Gate (4 pages)
1551	CD54/74HC10, CD54/74HCT10	High-Speed CMOS Logic, Triple 3-Input NAND Gate (4 pages)
1475	CD54/74HC11, CD54/74HCT11	High-Speed CMOS Logic, Triple 3-Input AND Gate (4 pages)
1781	CD54/74HC14, CD54/74HCT14	High-Speed CMOS Logic, He Inverting Schmitt Trigger (4 pages)
1601	CD54/74HC20, CD54/74HCT20	High-Speed CMOS Logic, Dua 4-Input NAND Gate (4 pages)
1782	CD54/74HC21, CD54/74HCT21	High-Speed CMOS Logic, Dua 4-Input AND Gate (4 pages)
1648	CD54/74HC27, CD54/74HCT27	Triple 3-Input NOR Gate (4 pages)
1652	CD54/74HC30, CD54/74HCT30	High-Speed CMOS Logic, 8-Input NAND Gate (4 pages)
1643	CD54/74HC32, CD54/74HCT32	High-Speed CMOS Logic, Quad 2-Input OR Gate (4 pages)
1689	CD54/74HC42, CD54/74HCT42	High-Speed CMOS Logic, BCD to Decimal Decoder (1-of-10) (4 pages)
1721	CD54/74HC73, CD54/74HCT73	Dual J-K Flip-Flop with Reset Negative-Edge Trigger (5 pages)
1476	CD54/74HC74, CD54/74HCT74	High-Speed CMOS Logic, Dua D Flip-Flop with Set and Rese Positive-Edge Trigger (5 pages)
1666	CD54/74HC75, CD54/74HCT75	Dual 2-Bit Bistable Transparent Latch (5 pages)
1770	CD54/74HC85, CD54/74HCT85	High-Speed CMOS Logic, 4-B Magnitude Comparator (6 pages)



AnswerFAX		
DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
1644	CD54/74HC86, CD54/74HCT86	High-Speed CMOS Logic, Quad 2-Input EXCLUSIVE - OR Gate (4 pages)
1849	CD54/74HC93, CD54/74HCT93	High-Speed CMOS Logic, 4-Bit Binary Ripple Counter (5 pages)
1722	CD54/74HC107, CD54/74HCT107	High-Speed CMOS Logic, Dual J-K Flip-Flop with Reset (5 pages)
1667	CD54/74HC109, CD54/74HCT109	High-Speed CMOS Logic, Dual J-K Flip-Flop with Set and Reset (5 pages)
1843	CD54/74HC112, CD54/74HCT112	High Speed CMOS Logic, Dual J-K Flip-Flop with Set and Reset (5 pages)
1708	CD54/74HC123, CD54/74HCT123, CD54/74HC423, CD54/74HCT423	High-Speed CMOS Logic, Dual Retriggerable Monostable Multivibrators with Resets (6 pages)
1771	CD54/74HC125, CD54/74HCT125	High-Speed CMOS Logic, Quad Buffer; 3-State (5 pages)
1772	CD54/74HC126, CD54/74HCT126	High-Speed CMOS Logic, Quad Buffer; 3-State (5 pages)
1649	CD54/74HC132, CD54/74HCT132	High-Speed CMOS Logic, Quad 2-Input NAND Schmitt Trigger (4 pages)
1886	CD54/74HC137, CD54/74HCT137, CD54/74HC237, CD54/74HCT237	High-Speed CMOS Logic, 3-to-8 Line Decoder/ Demultiplexer with Address Latches (8 pages)
1477	CD54/74HC138, CD54/74HCT138, CD54/74HC238, CD54/74HCT238	High-Speed CMOS Logic, 3-to- 8 Line Decoder/Demultiplexer Inverting and Non-Inverting (5 pages)
1545	CD54/74HC139, CD54/74HCT139	High-Speed CMOS Logic, Dual 2-to-4 Line Decoder/ Demultiplexer (5 pages)
1773	CD54/74HC147, CD54/74HCT147	High-Speed CMOS Logic, 10-to-4-Line Priority Encoder (5 pages)
1645	CD54/74HC151, CD54/74HCT151	High-Speed CMOS Logic, 8-Input Multiplexer (5 pages)
1774	CD54/74HC153, CD54/74HCT153	High-Speed CMOS Logic, Dual 4-Input Multiplexer (5 pages)
1657	CD54/74HC154, CD54/74HCT154	High-Speed CMOS Logic, 4-to-16 Line Decoder/ Demultiplexer (6 pages)
1642	CD54/74HC157, CD54/74HCT157, CD54/74HC158, CD54/74HCT158	High-Speed CMOS Logic, Quad 2-Input Multiplexers (5 pages)

AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
1550	CD54/74HC/ HCT160, CD54/ 74HC/HCT161, CD54/74HC/HCT162, CD54/74HC/HCT163	High-Speed CMOS Logic, Presettable Counters (10 pages)
1658	CD54/74HC164, CD54/74HCT164	High-Speed CMOS Logic, 8-Bit Serial-In/Parallel-Out Shift Register (5 pages)
1672	CD54/74HC165, CD54/74HCT165	High-Speed CMOS Logic, 8-Bit Parallel-In/Serial-Out Shift Register (6 pages)
1501	CD54/74HC166, CD54/74HCT166	High-Speed CMOS Logic, 8-Bit Parallel-In/Serial-Out Shift Register (6 pages)
1641	CD54/74HC173, CD54/74HCT173	High-Speed CMOS Logic, Quad D-Type Flip-Flop, 3-State Positive-Edge Triggered (6 pages)
1608	CD54/74HC174, CD54/74HCT174	High-Speed CMOS Logic, Hex D-Type Flip-Flop with Reset (5 pages)
1474	CD54/74HC175, CD54/74HCT175	High-Speed CMOS Logic, Quad D Flip-Flop with Reset (5 pages)
1829	CD54/74HC181, CD54/74HCT181	High-Speed CMOS Logic, 4-Arithmetic Logic Unit (6 pages)
1830	CD54/74HC182, CD54/74HCT182	High Speed CMOS Logic, Look Ahead Carry Generator (1 pages) Obsolete
1662	CD54/74HC190, CD54/74HCT190, CD54/74HC191, CD54/74HCT191	High-Speed CMOS Logic, Presettable Synchronous 4-Bit Up/Down Counters (9 pages)
1674	CD54/74HC192, CD54/74HCT192, CD54/74HC193, CD54/HCT193	High-Speed CMOS Logic, Presettable Synchronous 4-Bit Up/Down Counters (10 pages)
1668	CD54/74HC194, CD54/74HCT194	High-Speed CMOS Logic, 4-Bit Bidirectional Universal Shift Register (6 pages)
1482	CD54/74HC195, CD54/74HCT195	High-Speed CMOS Logic, 4-Bit Parallel Access Register (6 pages)
1670	CD54/74HC221, CD54/74HCT221	High-Speed CMOS Logic, Dual Monostable Multivibrator with Reset (7 pages)
1656	CD54/74HC240, CD54/74HC241, CD54/74HC244, CD54/74HCT240, CD54/74HCT241, CD54/74HCT244	High-Speed CMOS Logic, Octal Buffer/Line Drivers, 3-State (6 pages)



AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
1488	CD54/74HC242, CD54/74HCT242, CD54/74HC243, CD54/74HCT243	High-Speed CMOS Logic, Quad-Bus Transceiver with 3-State Outputs (6 pages)
1651	CD54/74HC245, CD54/74HCT245	High-Speed CMOS Logic, Octal-Bus Transceiver, 3-State, Non-Inverting (5 pages)
1489	CD54/74HC251, CD54/74HCT251	High-Speed CMOS Logic, 8-Input Multiplexer; 3-State (6 pages)
1673	CD54/74HC253, CD54/74HCT253	High-Speed CMOS Logic, Dual 4-Input Multiplexer (5 pages)
1650	CD54/74HC257, CD54/74HCT257	High-Speed CMOS Logic, Quad 2-Input Multiplexer with 3-State Non-Inverting Outputs (4 pages)
1775	CD54/74HC258, CD54/74HCT258	High-Speed CMOS Logic, Quad 2-Input Multiplexer with 3-State Inverting Outputs (5 pages)
1727	CD54/74HC259, CD54/74HCT259	High-Speed CMOS Logic, 8-Bit Addressable Latch (7 pages)
1479	CD54/74HC273, CD54/74HCT273	High-Speed CMOS Logic, Octal D Flip-Flop with Reset (5 pages)
1669	CD54/74HC280, CD54/74HCT280	High-Speed CMOS Logic, 9-Bit Odd/Even Parity Generator/Checker (4 pages)
1848	CD54/74HC283, CD54/74HCT283	High-Speed CMOS Logic, 4-Bit Binary Full Adder With Fast Carry (5 pages)
1852	CD54/74HC297, CD54/74HCT297	High-Speed CMOS Logic, Digital Phase-Locked-Loop (7 pages)
1485	CD54/74HC299, CD54/74HCT299	High-Speed CMOS Logic, 8-Bit Universal Shift Register; 3-State (7 pages)
1690	CD54/74HC354, CD54/74HCT354, CD54/74HC356, CD54/74HCT356	High-Speed CMOS Logic, 8-Input Multiplexer/Register, 3-State (10 pages)
1539	CD54/74HC365, CD54/74HCT365, CD54/74HC366, CD54/74HCT366	High-Speed CMOS Logic, Hex Buffer/Line Driver, 3-State Non-Inverting and Inverting (5 pages)
1538	CD54/74HC367, CD54/74HCT367, CD54/74HC368, CD54/74HCT368	High-Speed CMOS Logic, Hex Buffer/Line Driver, 3-State (5 pages)
1679	CD54/74HC373, CD54/74HCT373, CD54/74HC573, CD54/74HCT573	High-Speed CMOS Logic, Octal Transparent Latch, 3-State Output (6 pages)

AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
1663	CD54/74HC374, CD54/74HCT374, CD54/74HC574, CD54/74HCT574	High-Speed CMOS Logic, Octal D-Type Flip-Flop, 3-State Positive-Edge Triggered (5 pages)
1675	CD54/74HC377, CD54/74HCT377	High-Speed CMOS Logic, Octal D-Type Flip-Flop with Data Enable (6 pages)
1838	CD54/74HC390, CD54/74HCT390	High-Speed CMOS Logic, Dual Decade Ripple Counter (6 pages)
1653	CD54/74HC393, CD54/74HCT393	High-Speed CMOS Logic, Dual 4-Stage Binary Counter (5 pages)
1599	CD54/74HC533, CD54/74HCT533, CD54/74HC563, CD54/74HCT563	High-Speed CMOS Logic, Octal Inverting Transparent Latch, 3-State Outputs (6 pages)
1640	CD54/74HC534, CD54/74HCT534, CD54/74HC564, CD54/74HCT564	High-Speed CMOS Logic, Octal D-Type Flip-Flop, 3-State, Inverting Positive-Edge Triggered (5 pages)
1659	CD54/74HC540, CD54/74HCT540, CD54/74HC541, CD54/74HCT541	High-Speed CMOS Logic, Octal Buffer and Line Drivers 3-State (5 pages)
1828	CD54/74HC583, CD54/74HCT583	High-Speed CMOS Logic, 4-Bit BCD Full Adder with Fast Carry (5 pages)
1915	CD54/74HC597, CD54/74HCT597	High Speed CMOS Logic, 8-Bit Shift Register with Input Storage (8 pages)
1677	CD54/74HC640, CD54/74HCT640, CD54/74HC643, CD54/74HCT643	High-Speed CMOS Logic, Octal 3-State Bus Transceivers (5 pages)
1664	CD54/74HC646, CD54/74HCT646, CD54/74HC648, CD54/74HCT648	High-Speed CMOS Logic, Octal Bus Transceiver/ Register, 3-State (7 pages)
2229	CD54/74HC651, CD54/74HC652, CD54/74HCT651, CD54/74HCT652	Octal-Bus Transceiver/ Registers, 3-State (7 pages)
1660	CD54/74HC670, CD54/74HCT670	High-Speed CMOS Logic, 4 x 4 Register File (7 pages)
1646	CD54/74HC688, CD54/74HCT688	High-Speed CMOS Logic, 8-Bit Magnitude Comparator (4 pages)
1776	CD54/74HC4002, CD54/74HCT4002	High-Speed CMOS Logic, Dual 4-Input NOR Gate (4 pages)
1678	CD54/74HC4015, CD54/74HCT4015	High-Speed CMOS Logic, Dual 4-Stage Static Shift Register (6 pages)





AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
1917	CD54/74HC4016, CD54/74HCT4016	High-Speed CMOS Logic, Quad Bilateral Switch (7 pages)
1639	CD54/74HC4017, CD54/74HCT4017	High-Speed CMOS Logic, Decade Counter/Divider with 10 Decoded Outputs (6 pages)
1484	CD54/74HC4020, CD54/74HCT4020	High-Speed CMOS Logic, 14-Stage Binary Counter (5 pages)
1683	CD54/74HC4024, CD54/74HCT4024	High-Speed CMOS Logic, 7-Stage Binary Ripple Counter (5 pages)
1483	CD54/74HC4040, CD54/74HCT4040	High-Speed Logic, 12-Stage Binary Counter (5 pages)
1854	CD54/74HC4046A, CD54/74HCT4046A	High-Speed CMOS Logic, Phase-Locked-Loop with VCO (17 pages)
1543	CD54/74HC4049, CD54/74HC4050	High-Speed CMOS Logic, Hex Buffers, Inverting and Non- Inverting (4 pages)
1676	CD54/74HC4051, CD54/74HCT4051, CD54/74HC4052, CD54/74HCT4052, CD54/74HC4053, CD54/74HCT4053	High-Speed CMOS Logic, Analog Multiplexers/ Demultiplexers (9 pages)
1853	CD54/74HC4059, CD54/74HCT4059	High-Speed CMOS Logic, CMOS Programmable Divide- by-"N" Counter (7 pages)
1654	CD54/74HC4060, CD54/74HCT4060	High-Speed CMOS Logic, 14-Stage Binary Counter with Oscillator (6 pages)
1777	CD54/74HC4066, CD54/74HCT4066	High-Speed CMOS Logic, Quad Bilateral Switch (6 pages)
1783	CD54/74HC4067, CD54/74HCT4067	High-Speed CMOS Logic, 16-Channel Analog Multiplexer/Demultiplexer (6 pages)
1778	CD54/74HC4075, CD54/74HCT4075	High-Speed CMOS Logic, Triple 3-Input OR Gate (4 pages)
1779	CD54/74HC4094, CD54/74HCT4094	High-Speed CMOS Logic, 8-Stage Shift-and-Store Bus Register - 3-State (7 pages)
1916	CD54/74HC4316, CD54/74HCT4316	High-Speed CMOS Logic, Quad Analog Switch with Level Translation (7 pages)
2145	CD54/74HC4351, CD54/74HCT4351, CD54/74HC4352, CD54/74HCT4352, CD54/74HC4353, CD54/74HCT4353	Analog Multiplexers/ Demultiplexers With Latch (13 pages)

AnswerFAX DOCUMENT		
NUMBER	PART NUMBER	DESCRIPTION
1823	CD54/74HC4510, CD54/74HCT4510, CD54/74HC4516, CD54/74HCT4516	High-Speed CMOS Logic, Presettable Synchronous 4-Bit Up/Down Counters (10 pages)
1786	CD54/74HC4511, CD54/74HCT4511	High-Speed CMOS Logic, BCD-to-7 Segment Latch/ Decoder/Drivers (5 pages)
1597	CD54/74HC4514, CD54/74HCT4514, CD54/74HC4515, CD54/74HCT4515	High-Speed CMOS Logic, 4-to-16 Line Decoder/ Demultiplexer with Input Latches (6 pages)
1665	CD54/74HC4518, CD54/74HCT4518, CD54/74HC4520, CD54/74HCT4520	High-Speed CMOS Logic, Dual Synchronous Counters (6 pages)
1671	CD54/74HC4538, CD54/74HCT4538	High-Speed CMOS Logic Dual Retriggerable Precision Monostable Multivibrator (8 pages)
1822	CD54/74HC4543, CD54/74HCT4543	High-Speed CMOS Logic, BCD-to-7 Segment Latch/ Decoder/Driver for LCDs (6 pages)
2122	CD54/74HC7030, CD54/74HCT7030	64-Word x 9-Bit FIFO Register; 3-State (13 pages)
1872	CD54/74HC7038, CD54/74HCT7038	High-Speed CMOS Logic, 9-Bit Bus Transceiver with Latch (1 pages) Obsolete
	CD54/74HC7046A, CD54/74HCT7046A	Phase-Locked Loop with VCO and Lock Dectector (16 pages)
1780	CD54/74HC7266	High-Speed CMOS Logic, Quad 2-Input Exclusive-NOR Gate (4 pages)
	CD54/74HC40102, CD54/74HCT40102, CD54/74HC40103, CD54/74HCT40103	High-Speed CMOS Logic, 8-Stage Synchronous Down Counters (9 pages)
	CD54/74HC40104, CD54/74HCT40104	High-Speed CMOS Logic, 4-Bit Universal Bidirectional Shift Register (6 pages)
	CD54/74HC40105, CD54/74HCT40105	High-Speed CMOS Logic, 4-Bit x 16-Word FIFO Register (9 pages)
1655	CD54/74HCU04	High-Speed CMOS Logic, Hex Inverter (4 pages)
CD54 HC/HCT H	H-REL LOGIC DATA	SHEETS
3753	CD54HC00/3A, CD54HCT00/3A	Quad 2-Input NAND Gate (1 pages)
3754	CD54HC02/3A, CD54HCT02/3A	Quad 2-Input NOR Gate (1 pages)
3755	CD54HC03/3A, CD54HCT03/3A	Quad 2-Input NAND Gate (1 pages)

HARRIS SEMICONDUCTOR

AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
3756	CD54HC04/3A, CD54HCT04/3A	Hex Inverter (1 pages)
3757	CD54HC08/3A, CD54HCT08/3A	Quad 2-Input AND Gate (1 pages)
3758	CD54HC10/3A, CD54HCT10/3A	Triple 3-Input NAND Gate (1 pages)
3759	CD54HC11/3A, CD54HCT11/3A	Triple 3-Input AND Gate (1 pages)
3760	CD54HC14/3A, CD54HCT14/3A	Hex Inverting Schmitt Trigger (1 pages)
3761	CD54HC20/3A, CD54HCT20/3A	Dual 4-Input NAND Gate (1 pages)
3762	CD54HC21/3A, CD54HCT21/3A	Dual 4-Input AND Gate (1 pages)
3763	CD54HC27/3A, CD54HCT27/3A	Triple 3-Input NOR Gate (1 pages)
3764	CD54HC30/3A, CD54HCT30/3A	8-Input NAND Gate (1 pages)
3765	CD54HC32/3A, CD54HCT32/3A	Quad 2-Input OR Gate (1 pages)
3766	CD54HC42/3A, CD54HCT42/3A	BCD-to-Decimal Decoder (1-to-10) (1 pages)
3767	CD54HC73/3A	Dual J-K Flip-Flop with Set and Reset (1 pages)
3768	CD54HC74/3A, CD54HCT74/3A	Dual D Flip-Flop with Set and Reset (1 pages)
3769	CD54HC75/3A, CD54HCT75/3A	Quad Bistable Transparent Latch (1 pages)
3770	CD54HC85/3A, CD54HCT85/3A	4-Bit Magnitude Comparator (1 pages)
3771	CD54HC86/3A, CD54HCT86/3A	Quad 2-Input EXCLUSIVE-OR Gate (1 pages)
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9

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